analog dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing

Volume 23, Number 4, 1989

ANALOG DEVICES

Editor's Notes

INTERESTING READING

A survey we ran a few years ago told us you were interested in (among other things) information that would be of practical value in circuit and system design. We've continually sought to fulfill this interest (among others) in these pages and in books we've published, as well as in Analog Devices data sheets, seminars, application notes, and other media.

But we certainly don't have a monopoly on disseminating this kind of information. There are many other publications that provide helpful lore—and we frequently mention them in footnote references. Indeed, we consider it a responsibility to tell you about publications we encounter that impress us with their usefulness. There are two that we'd like to bring to your attention (or remind you of, if you're already aware of them.)

The first is a book, *The Art of Electronics*, second edition, by Horowitz and Hill.[1] In our opinion, it comes as close as any book we've seen to fulfilling the promise inherent in its title; it's a book we wish we had written. Naturally, it is large (1,124 pages); it is comprehensive—everything from voltage, current, and resistance to measurements and signal processing; it proceeds in logical and thorough order; it is written in a clear and friendly tone; it is illustrated by many practical tables—with surprisingly up-to-date manufacturers' data. It is written as though to educate the novice, but practicing engineers will encounter many useful tidbits they didn't know, hadn't thought about, or had long forgotten. For example:

> "Here's the craziest of them all: You forgot to wire up the V_{DD} pin on a CMOS chip, but the circuit works just fine! That's because it is being powered by one of its logic inputs (via the input-protection diodes from the input to the V_{DD} line in the chip). You might get away with this for a long time, but suddenly the circuit reaches a state where all the logic inputs to the chip are simultaneously LOW; the chip loses power and forgets its state . . ."

It is profusely illustrated with diagrams and waveforms and incorporates a unique feature: exercises consisting of assortments of self-explanatory "Circuit ideas" and "Bad circuits."

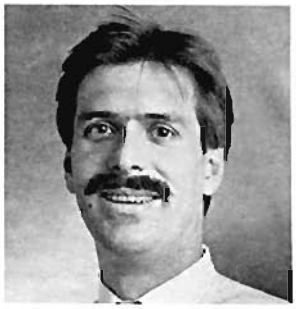
Our other notable encounter is with EDN magazine's highly useful 12-part series, "Troubleshooting Analog Circuits," by our former colleague, Bob Pease.[2] You've probably encountered it if you read EDN even sporadically during 1989. He starts with philosophy, goes on to equipment, then covers components, capacitors, material and assembly problems, active components, transistors, op-amp circuits, spurious oscillations, the a:d boundary, power components, and a final wrapup. We suspect that this series will reappear fairly soon as a book. Get it.

Dan Sheingold

[1]Paul Horowitz and Winfield Hill, *The Art of Electronics*, 2nd edition. Cambridge (UK): Cambridge University Press, 1989.

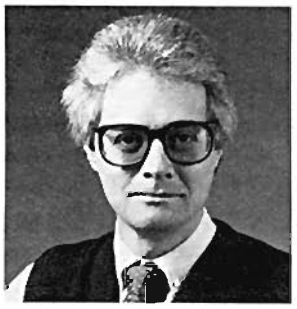
[2]Bob Pease, "Troubleshooting Analog Circuits", *EDN*, 1989 series: Jan. 5, 19; Feb. 2, 16; March 2; Aug. 3, 17; Sept. 1, 14, 28; Oct. 12, 26.

THE AUTHORS



Bill Gotschewski (page 3), Product Line Marketing Manager for Analog Devices' Microelectronics Division, in Wilmington, Massachusetts, has a BSEE from the University of Illinois. Previously he was a design engineer for MA/COM and joined Analog Devices in 1984. He enjoys his new baby girl, a variety of sports, and the Cubs.

Stephan Goldstein (page 8), designer of the AD1330, is a Senior Applications Engineer for all product lines at ADI's Microelectronics Division. Prior to this, he was a designer for 7 1/2 years; his other data-acquisition product designs include the AD367 and the AD386. He has BS and MS degrees in Electrical Engineering from MIT. His hobbies include target shooting, piano playing, and lepidoptera (i.e., collecting butterflies).



Tom Kelly (page 10), who designed the μMAC-1050 hardware, is a staff engineer for the Analog Devices Industrial Products Division, in Norwood, Massachusetts. He joined ADI's MACSYM group in 1977 after obtaining a BSEE from Rutgers University, College of Engineering. He has designed products for the MACSYM, RTI, and μMAC product lines.

Raouf Bortcosh (page 10), a Staff Engineer for Analog Devices' Industrial Products Division, is responsible for all programmable μMAC-series software. He developed the firmware for the μMAC-1050. Raouf has a BSEE, an MSEE, and an MSEM from Northeastern University. He joined Analog Devices in 1979.

Bill Schweber (page 3) is a Senior Technical Marketing Engineer and Contributing Editor to *Analog Dialogue*, responsible for many of the articles in this issue. His photo and a biographical sketch appeared in volume 23, number 3.

(More authors on page 22)

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HIGH SPEED AUTOMATIC TESTING FOR ADVANCED COMPONENTS

Pin Drivers, Comparators, DACs, and Active Loads Have Key Roles

Size, Speed, Power, Accuracy, and Repeatability are Constraints

by Bill Gotschewski and Bill Schweber

Designers of automatic test equipment (ATE) systems for advanced components have always had a dilemma: in order to test the newest, fastest, most precise products, they themselves need components that are even better than those they are testing. The unique design constraints of ATE add to the difficulties of assembling a system for testing high-speed, high-pin-count devices.

The electrical interface between the device under test (DUT) and the rest of the ATE system is the *pin electronics*, a complex subsystem containing the functions needed to source precise signals to the DUT pins as well as measure DUT-generated signals. There is an identical—or nearly so—pin electronics circuit for each active pin of the DUT, arranged in a circle around the DUT at the test head to maximize achievable density and partially equalize propagation delays between pin electronics and the DUT.

The heart of the pin electronics is the pin driver. This device must produce highly repeatable, low-jitter pulses with precisely set amplitude and slew rate for the DUT. The pin-driver timing is set digitally; its amplitude is determined by analog control voltages. Because of the high speeds of pin drivers—a 100-MHz repetition rate corresponds to a 5-ns pulse width—the driver and DUT are typically interconnected by a 50-Ω transmission line. The pin driver can be digitally disconnected via a high-impedance three-state output mode, needed when the DUT has an input/output pin (two modes) that must be tested without physically disconnecting the driver.

Figure 1, a typical pin-electronics block diagram, shows the variety of devices needed for the complete function. Under control of the test computer and dedicated hardware, desired data patterns must be generated for simultaneous application to DUT inputs; at the same time, appropriate DUT outputs must be captured and measured. For complete parametric testing, signal levels must be

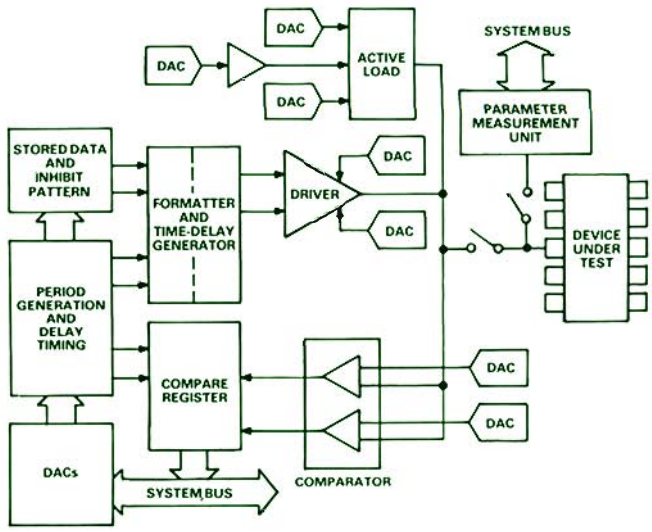
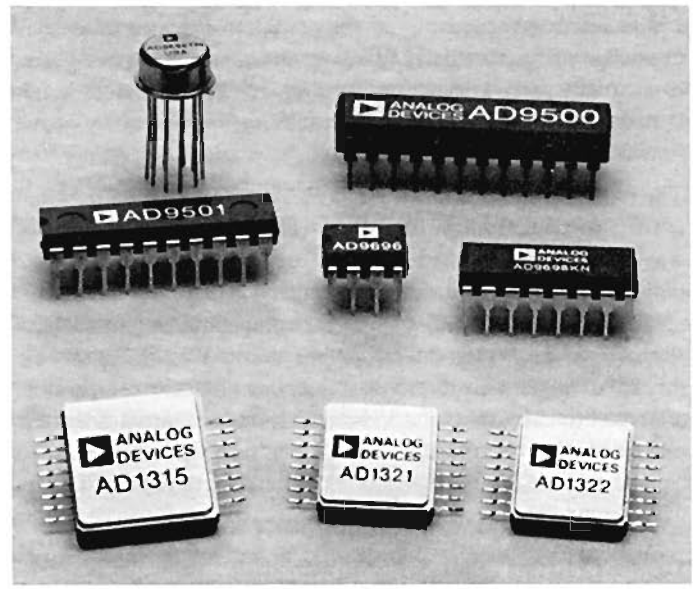


Figure 1. Typical pin-electronics block diagram. All items shown may recur for each driven pin in high-performance systems.



precisely varied by the test program to determine maximum and minimum performance boundaries.

The complete pin-electronics function requires many digital-to-analog converters (DACs) for setting levels. The driver itself uses two DACs for high and low levels. The active load—which emulates actual circuit loads—requires three DACs to program the source current, sink current, and the threshold (commutation) voltage between current sourcing and -sinking modes.

Although Figure 1 shows DACs setting key levels, many testers now use rapidly refreshed *sample/hold* circuits—driven by a shared, precise DAC. The S/H amplifier is used in *data distribu-*

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tion instead of data acquisition, i.e., the S/H *holds* a digitally determined value during the test to establish a quasi-steady-state value instead of capturing an unknown signal value prior to digitizing it.[1]

Unavoidable time skew occurs between signals from the many drivers as they reach the DUT. This is due to different path lengths (and therefore delays), as well as propagation delays within active components. To compensate for this, a time-delay de-skewing circuit or delay line is included with each pin's electronics. The precise delay time must be set with high resolution; it is determined during the system calibration cycles or by actual test.

The pulse output of a DUT pin is measured to provide rise- and fall times (time from 10 to 90 per cent of up- or downswing), amplitudes, slew rate, and related information. For the short time periods associated with these parameters, the measurements are made using pairs of comparators: the comparator output changes state when the waveform under observation crosses a specific threshold value. The threshold values for all these comparators are established by DACs or S/H circuits, under control of the test computer. The comparator outputs, in turn, are connected to circuits that measure the period between changes in output states of the comparators.

DESIGN CHALLENGES

The designer's task is made more difficult by many simultaneous and often conflicting demands, as ATE speeds reach 200 MHz (and beyond) and DUT package content increases:

- high-speed signal transitions are affected by parasitic inductance and capacitance, which slow the transitions and affect waveshape fidelity.
- noise glitches induced by high-speed signals corrupt signals in nearby wiring; although decoupling, short leads, and ground planes are a minimum line of defense against these, more advanced techniques, such as differential signal paths, may also be required.
- accuracy in measurement requires components whose dynamic performance is predictable and stable with time and temperature. For a 200-MHz pin driver, the leading-edge-to-trailing-edge matching specification should be better than 200 ps. Low *dispersion* (variation in propagation delay as a function of the input signal swing) reduces skewing and makes compensation more precise; for example, low dispersion is critical in memory testers, to minimize the need for compensating delay lines on their many data pins. Dispersion matching should be close, both within a device and from device to device, for ease of replacement and calibration.
- slew rates must also be controlled (2 V/ns for the 200-MHz driver) for performance consistency.
- undershoot and overshoot of the pin-driver output must be limited in amplitude.
- the DUT must be tested at its normal operating voltages—and stressed beyond these values, so the ATE components must typically be capable of functioning with signals from −2 to +7 volts.
- *mixed-signal* testing imposes *additional* requirements for signal linearity, ramping, precision, and distortion for typically 20 out of 64 DUT pins.

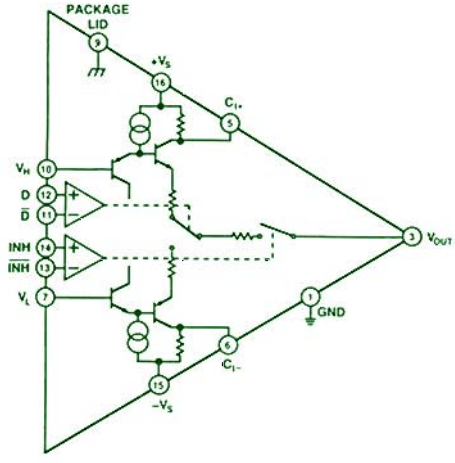


Figure 2. Block diagram of AD1321/AD1322 Pin Drivers.

The constraints are not solely electronic; electromechanical factors are also significant:

- test-head pin counts are increasing from 64 (typically) to 512 pins, requiring that more electronic circuitry be packed into the limited available space; using a larger test head means more propagation-delay uncertainty, timing mismatches, and corresponding inaccuracies.
- power consumption of the high-speed circuitry is relatively high, exceeding 3 watts per pin; cooling the large number of densely populated pin-electronic circuits is difficult.
- power consumption and heating, along with other factors, affect reliability, which must be very high in a multi-million dollar test machine; users expect satisfactory uptime and test throughput.
- the layout of the test head must maintain signal fidelity; transmission-line impedances must be held constant to minimize signal reflections between DUT and pin electronics.
- and, of course, cost becomes a significant factor when the per-pin cost is multiplied by the large number of pins.

COMPONENTS FOR ATE

A complete ATE test-head design requires an appropriate mix of high-speed, high-performance components that are small enough to provide the needed functional density. Analog Devices provides a wide selection of components, based on various IC process technologies and logic families, to provide appropriate choices for ATE.

AD1322 and AD1321* Pin Drivers: These monolithic high-speed pin drivers, with respective speeds of 200 MHz (2.5-ns pulse width) and 100 MHz (5-ns pulse width) have the functions depicted in Figure 2. They include *inhibit-mode* circuitry, which can effectively disconnect their outputs from the pin. Their output is designed to stimulate ECL, TTL, and CMOS logic families. They are housed in a unique surface-mount package—an ultra-small 16-pin hermetically sealed enclosure (Figure 3), which combines the necessary electrical performance with high packaging density and long-term reliability.

With +10 and −5.2-volt power supplies, the output level of the

[1]See Chapter 3, "Data Distribution," in *Analog-Digital Conversion Handbook*, 3rd Edition (1986) published by Prentice-Hall and available from Analog Devices. Use book-order card.

*Use the reply card for technical data.

Figure 3. Packaging of the AD1321/AD1322.

AD1322 (and AD1321) can swing from –2 to +7 volts, with a minimum settable span of 100 mV. High- and low levels are set by analog inputs, V_H and V_L, which require less than 200 μA of bias current, so a single control input can set V_H or V_L for many drivers wired in parallel. Thermal variation in propagation delay with duty cycle of applied pulses is negligible.

Leakage in the high-impedance output state is less than 100 nA, and output charge transfer when switched into this three-state mode is less than 5 pC. Both the Data and Inhibit inputs can be driven by single-ended TTL or CMOS logic sources—or by differential ECL for higher speed and precision. Respective prices are $40 and $78 for the AD1321 and AD1322 in 1,000s.

AD1315* Active Load with Inhibit mode: Housed in an ultrasmall 16-pin hermetically sealed package, this current-switching dynamic load (Figure 4) is designed to force the DUT pin to sink or source up to ±50 mA. The programmable ranges for both high- and low current (I_{OH} and I_{OL}) are independently set by external voltages, using internal V-to-I converters; the 50-kΩ loading of the control input pin is essentially negligible. In 1,000s, the AD1315 is priced at $35.

The transition from I_{OH} to I_{OL} occurs automatically when the DUT pin voltage crosses a threshold (commutation) voltage, programmable from –2 to +7 volts to meet requirements of the major logic families. Leakage is less than 200 nA in the Inhibit (off) mode, which is controlled by high-speed differential inputs —compatible with both ECL and TTL/CMOS. Switching time from either active state to Inhibit mode is less than 1.5 ns, freeing the test system to switch the pin of the DUT quickly to the next stimulus without a long wait for the load to clear (often microseconds in the past).

AD1317* Dual Comparator with Latch: This ultrafast dual voltage comparator combines high speed (propagation delay of 2.5 ns) with high dc accuracy—5-mV offset and 20-μV/°C drift. Its differential input stage has a common-mode range of –2 to +7 volts; the complementary outputs are ECL-compatible. The Latch function allows it to be used in either sample/hold mode or with hysteresis. An Inhibit control forces the comparator into a high-impedance-input mode, which effectively removes it from the measurement path, reducing its input bias current from 10 μA to picoamp values. Dispersion is 100 ps for slew rates of 0.5 V/ns to 3.5 V/ns and 0.05-to-5-volt overdrive. This comparator, available soon, will be priced at $21 in 1,000s.

AD96685 and AD96687* Single and Dual Latching Comparators: These comparators (*Analog Dialogue* 21-2), providing either single or dual units, offer typical propagation delay of 2.5 ns (3.5 ns maximum) and propagation-delay dispersion of 50 ps. Operating from +5 and –5.2-V supplies, they have ECL-compatible digital outputs. Input range is from –2.5 to +5 volts, with maximum offset of 3 mV over the full operating temperature range; CMR is 80 dB. A latch allows the output state to track the input condition or hold an existing output until reset.

AD9696 and AD9698* (see page 17 of this issue) are the fastest available single and dual **TTL Comparators**; they have 4.5-ns propagation delay and 200-ps delay dispersion.

AD9686* Comparator: This monolithic *TTL* latching comparator (*Analog Dialogue* 22-1) features only 7 ns of propagation delay. In addition to its complementary TTL outputs, it has a latch-enable control line (with 2-ns maximum setup time) for very high speed voltage comparison in the TTL domain. Requiring +5 and –6-V supplies, the AD9686 has offset voltage of 2 mV, drift of 10 μV/°C, and 85-dB common-mode rejection.

AD7228* Octuple DAC: Designed for very high functional density, the monolithic TTL/CMOS-compatible AD7228 (*Analog Dialogue* 21-2) houses eight independent voltage-output 8-bit DACs in a single 0.3" wide 24-pin DIP (or PLCC or LCCC equivalent). The eight DACs share a common external reference; data is loaded through an eight-bit input port, and three address bits select the DAC to be updated (each DAC has its own data latch). [Note: Besides the AD7228, a wide variety of multiple DACs are available, including 12-bit quad DACs.]

With dual supplies, the reference can be between +2 and +10 V; single supply operation is also specified. Each output buffer amplifier can develop up to +10 V across a 2-kΩ load.

AD9500* (and AD9501):* These monolithic **Digitally Programmable Delay Generators** are designed to delay an input signal edge by an interval proportional to an 8-bit word—useful for pulse de-skewing, alignment, and synchronization. The *ECL-compatible AD9500* (*Analog Dialogue* 22-1) offers full-scale range of 2.5 ns to 100 μs, with 10-ps resolution on the smallest range. The *TTL- and CMOS-compatible AD9501* (*Analog Dialogue* 23-2) operates from a single +5-V supply and has full-scale range from 2.5 ns to 10 μs, with the same 10-ps resolution but greater internal propagation delay.

The full-scale range of programmable delays is set by an external resistor and capacitor. The 8-bit control word sets the time delay as a fraction of the full-scale range. When triggered by the leading edge of an input pulse, the device's output is delayed by a time interval equal to the selected value plus the propagation delay.

The AD13XX parts described in this article were designed by Barry Hilton, Paul Hilton, and Doug Babcock, working with Technical Group Leader Curtis Davis; all are at Analog Devices' Microelectronics Division, Wilmington, MA.

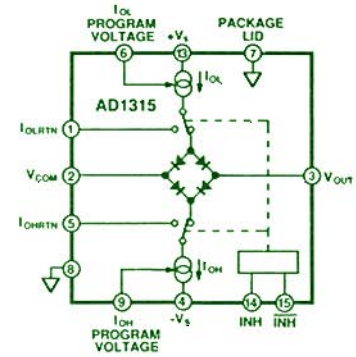


Figure 4. Functional diagram of the AD1315 Active Load. Note that I_{OH}, flowing in the direction indicated, is a *positive* current from the DUT (output voltage *high*).

12-BIT DACS OPTIMIZED FOR DIRECT DIGITAL SYNTHESIS

AD9712 (100 MSPS), AD9713 (80 MSPS) Generate Precise Waveforms

Low Glitch, Wide Spurious-Free Dynamic Range are Key Attributes

The AD9712 (ECL-compatible) and AD9713 (TTL-compatible) 12-bit digital-to-analog converters* are optimized for arbitrary waveform generation and direct digital synthesis. Capable of accepting new data words at up to 100 and 80 megasamples per second (MSPS) respectively, both monolithic devices provide the low glitch, low data-skew, and high spurious-free dynamic-range (SFDR) specifications needed for those applications.

In waveform generation and direct digital synthesis, absolute accuracy and related dc specifications are not as critical as dynamic specs. The AD9712 and AD9713 settle to ±1 LSB in less than 30 ns, with glitch impulse typically less than 100 pV-s. Both DACs maintain spec'd linearity without factory or user trim.

Spurious-Free Dynamic Range: SFDR is the logarithmic measure (dBc) of the ratio of the fundamental amplitude to the worst spurious component in the output spectrum (not necessarily a harmonic). For the AD9712, Figure 1 shows SFDR as a function of analog output frequency for encode rates of 25 and 100 MSPS. The AD9712's typical SFDR is 60 dBc with an update rate of 25 MHz for a 5-MHz sine wave; for the AD9713—under the same conditions—the SFDR is 55 dBc.

Internal Architecture: Both AD9712 and AD9713 are internally identical—with one difference: the AD9712 uses single-ended ECL-compatible inputs designed to match 10K ECL device thresholds for all digital inputs; the AD9713 adds a TTL level-shifter at each input.

The data inputs are applied to the DAC in parallel; the four MSBs are decoded to fifteen "thermometer code" segments for improved differential linearity. The remaining eight LSBs pass through time-delay equalizing circuitry, to minimize both bit-to-bit data skew and setup and hold times when subsequent inputs are latched. (Without this delay equalization, skew caused by the decoding circuits would increase glitch impulse). The internal latch circuitry synchronizes data inputs when the *Latch Enable* pin is pulsed.

Data from the latches goes to a switch network, which controls complementary current outputs. The four MSBs, decoded into 15

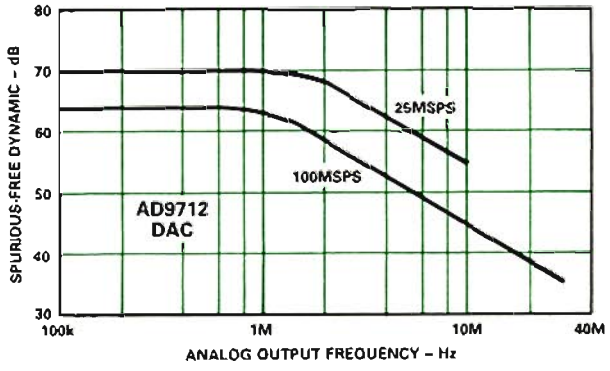
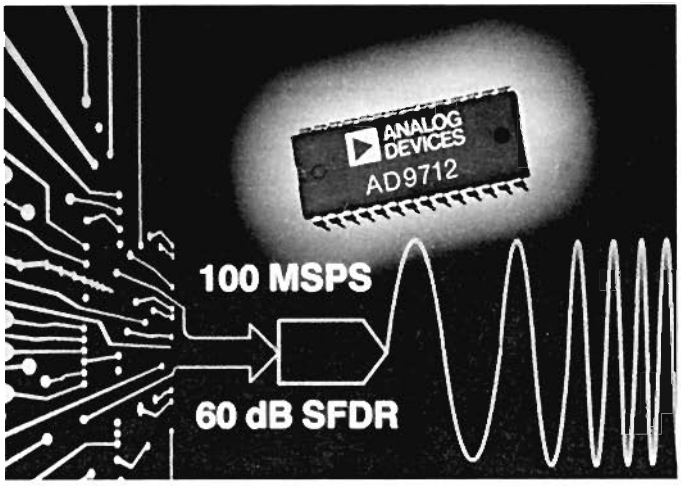


Figure 1. AD9712 dynamic range versus frequency of analog output.

*Use the reply card for technical data.



lines, drive matched current sources; data bits D5 and D6 control weighted current sources; and the remaining six LSBs (D7-D12) are applied to an R-2R network. This segmentation ensures specified linearity without trimming and reduces frequency-domain errors due to glitch impulse. In proportion to the digital input code value, current is steered to either the current-sum output or its complement; the sum of the two current outputs is always equal to the full-scale output current (less one LSB).

Analog Output Flexibility: Output level is set by the internal band-gap reference and an external resistor; nominal full-scale output current of 20.48 mA swings the output from 0 to −1.024 volts across a 50-Ω load resistor. The internal reference has a tolerance of ±20 % and drift of 440 μV/°C. For applications which require greater dc accuracy and stability, an external reference, such as the 1.2-volt AD589 (±10 ppm/°C drift) can be connected in place of the internal reference. As an alternative to resistive loading, a separate I/V converter (i.e., an op-amp circuit) may be used to convert the output current to a voltage.

Multiplying d/a conversion is realized in two ways with the AD9712 and AD9713. The control amplifier will accept signals swinging from −0.1 to −1.2 V, with bandwidths up to 400 kHz, as a substitute for the internal or external fixed dc reference. When the reference input is driven directly, wider multiplying bandwidths—up to 40 MHz—are realized. In this mode, the control signal must be between −4 and −5.2 volts. A simple way to do this is to capacitively couple the ac signal into the reference input and establish the correct dc bias with a simple resistive divider between $-V_S$ and ground at the reference input.

Operation requires a single −5.2-volt supply for the ECL-compatible AD9712, while the TTL-compatible AD9713 also requires a +5-V supply. Power dissipation is less than 700 mW for the AD9712 and 726 mW for the AD9713. Both devices are available in 28-pin plastic DIP and PLCC, for operation from 0 to +70°C. Prices begin at $40 (100s) for both devices.

The AD9712 and AD9713 were designed by John Studders of Analog Devices Computer Labs Division, Greensboro, NC.

8-BIT ANALOG I/O PORT FOR POSITION MONITORING & CONTROL

CMOS AD7769 Has Two-Channel ADC and Two 2.5-μs Vout DACs

Monolithic Device Is Designed to Work with Positive-Only Supplies

by John Wynne

The AD7769* is a complete two-channel, 8-bit analog I/O port designed for easy interfacing to microprocessors, microcomputers, and DSP processors as a memory-mapped peripheral or I/O device. It contains a multiplexed two-channel 8-bit high-speed sampling a/d converter, a pair of fast-settling voltage-output 8-bit d/a converters, registers, an I/O bus, signal conditioning for the analog inputs and outputs, and control logic (Figure 1). It operates from positive power-supply voltages.

Its architecture, features, and speed make it ideal for use in head-positioning servos in Winchester disk systems—and equally suitable for microstepped floppy-disk head positioning, other closed-loop digital servo systems, and general-purpose 8-bit data acquisition.

Signal Conditioning: The offset (zero point) and span of the analog inputs, and the offset and span of the analog outputs, can be independently set by externally applied ground-referenced voltages, which could be derived from a system reference. This makes the AD7769 especially useful in disk drives, where only a positive supply rail is available and the ranges of the ADC and DACs must be referenced to a positive voltage.

In the scheme shown in Figure 2, the reference—which might be a 5-volt AD586, supplied from the +12-volt V_{DD}—drives the bias inputs of the DACs and ADC; and the voltage dividers comprising R1 & R2 and R3 & R4 establish the swings ($\pm V_{SWING}$) of the DAC outputs and ADC inputs, respectively. For example, a DAC-output division ratio of 0.6 would produce a ±3-volt full-scale swing about a +5-volt offset; the same division ratio for the ADC input stage would swing the offset binary output codes from 00 to FF (hex) for a 2 to 8-volt span, with code 80 at +5 volts.

A/D Converter: The a/d converter has differential nonlinearity and relative-accuracy error of ±1 LSB max, with no missing codes over temperature. Frequency response is typically within 0.1 dB, for a full-scale sine wave from dc to 200 kHz, with minimum SNR of 44 dB and maximum total harmonic distortion of –48 dB for a 100-kHz sine wave sampled at 400 ksps.

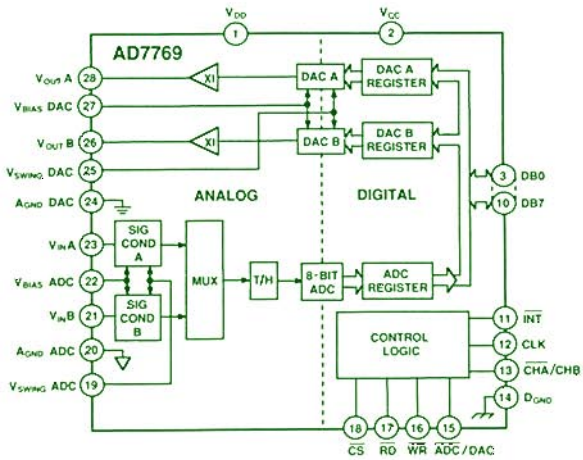
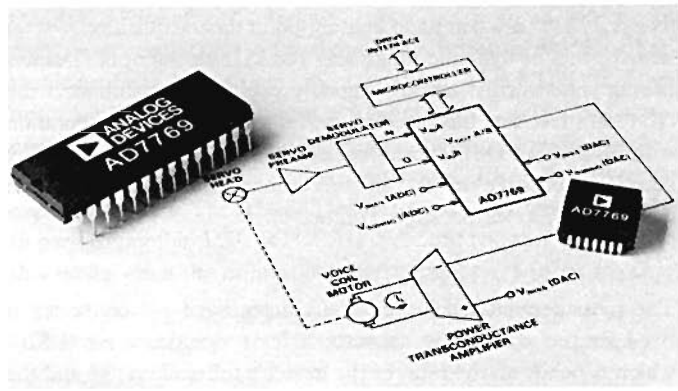


Figure 1. Block diagram of the AD7769.

*Use the reply card for technical data.



Typical dedicated servo control loop using the AD7769.

D/A Converters: The 8-bit DACs are guaranteed monotonic over temperature with maximum differential nonlinearity and relative-accuracy error of ±1 LSB. Signal-to-noise and total harmonic distortion are 44 dB min and –48 dB max for a 20-kHz sine wave sampled at 400 kHz. Settling time of voltage output is typically 2.5 μs (4 μs max) to within ±1/2 LSB of final value.

Interfacing: The AD7769 is easily interfaced to a standard 8-bit MPU bus via an 8-bit data port and standard microprocessor control lines. Timing is compatible with all modern μPs, with bus access and relinquish times less than 65 ns and Write pulse width less than 90 ns. An Interrupt output, set high on the falling edge of $\overline{RD}$ or $\overline{WR}$ to the ADC, goes low to signal the end of a conversion.

Two grades of the AD7769 are available: "J," for 0 to +70°C, and "A," for −40 to +85°C; the maximum error specifications for both grades are: ADC bias offset error, 2.5 LSB at +25°C, ±3.0 LSB over temperature; ADC to DAC bias offset match, ±2.5 LSB at +25°C, ±3.5 LSB over temperature; and DAC plus or minus full-scale error, ±1.5 LSB at +25°C. Package options are: 28-pin plastic DIP and 28-terminal PLCC. Prices (100s) begin at $13.00.

The AD7769 was designed by Philip Quinlan at Analog Devices BV, in Limerick, Ireland.

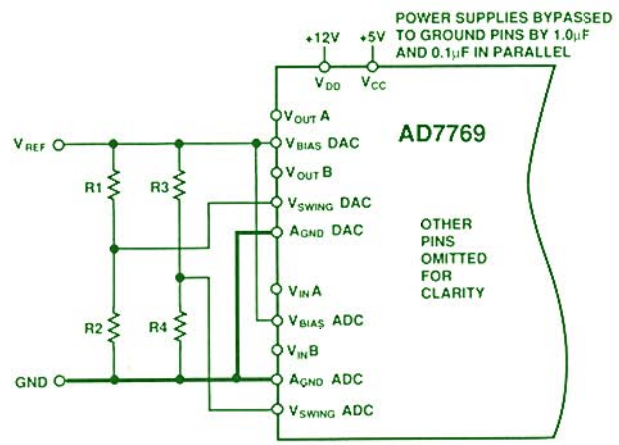


Figure 2. Typical reference connections to AD7769.

FLOATING-POINT DATA-ACQUISITION SYSTEM

AD1330 Provides 18-Bit Dynamic Range in Two Hybrid Packages Samples at up to 100 ksps; Transfers Data within 15 ns

by Stephan Goldstein

The AD1330* is a complete floating-point data-acquisition system with 18 bits of dynamic range and 100-kHz throughput. Besides having noteworthy analog signal-processing capabilities, the AD1330's fast data bus interface permits zero-wait-state operation with high-speed DSP microprocessors. Hybrid circuit technology makes it possible to fit all this functionality into just two hermetically-sealed packages (Figure 1).

WHAT IS FLOATING-POINT?

The measurement resolution of a conventional a/d converter is fixed by the size of the converter's least significant bit (LSB), which depends on the ratio of the device's full-scale range and the number of bits it can resolve. For example, a 12-bit ADC with a 10-volt signal range has a 2.44-mV LSB (10 V/2^{12}). To measure signals with wide dynamic range, LSB size can be reduced by increasing the number of bits of resolution; this costs increased conversion time because of an increase in the number of bit decisions and the time required for the internal signals to settle sufficiently to guarantee a correct decision. For example, the AD578L can complete a 12-bit conversion in just 3 μs, while the AD1377K requires 10 μs to perform a 16-bit conversion.

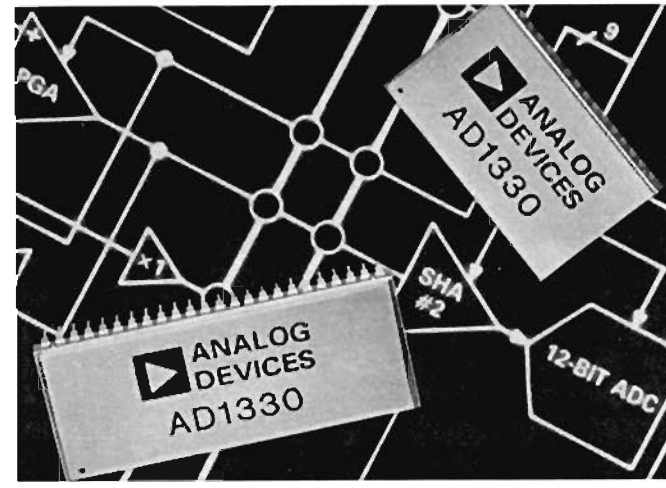
In some instances, very small changes in the input need to be resolved only when the signal is small; as it increases, the absolute measurement accuracy may be reduced without losing significant information. For instance, one may need to measure the input with an accuracy of better than 100 μV for signal levels below 100 mV, but 2 mV of resolution may be adequate when the input level rises to 2 V. In ratiometric applications, for example, only the relative values of measurements are important. An ADC in which the LSB weight varies in response to the input signal can meet this requirement and probably bypass the resolution/throughput barrier of more-conventional converters.

In the AD1330, the LSB size is changed by factors of two using a programmable-gain-amplifier ahead of the ADC. A nearly full-scale input would be passed through with unity gain, an input slightly below half-scale might see a gain of 2, etc., making the effective LSB smaller as the signal decreases in magnitude and increasing the overall measurement resolution for small inputs. (The size of the ADC's LSB is unchanged, but the added gain reduces the change in input signal required to cause a 1-LSB change in the ADC's output code.) Because of the binary weighting of gains, this amounts to moving the "binary point" of the ADC's output word, hence "floating point." The input can be reconstructed using the ADC's output code and the gain value used to obtain that result. In the AD1330, this technique provides an 18-bit dynamic range with 100-kHz throughput.

WHY USE FLOATING-POINT?

Two numerical examples illustrate the power of floating point. Suppose that a system's maximum allowable input signal is ±5 volts and that it must measure two signals with amplitudes of

*Use the reply card for a 20-page data sheet with details about the device's operation, interfacing, and signal-reconstruction techniques.



+267 μV and +2,670 μV. Signals in this range are amplified by a factor of 64 before processing by the AD1330's internal 12-bit ADC, so the effective LSB size is 38 μV, i.e., 10 V/(4,096×64), *equivalent to the LSB of an 18-bit converter*. The signal amplitudes are found to be 7 and 70 of these 38-μV LSBs, and their ratio (based on the AD1330's result) is equal to their true ratio: 0.1. For the same signals, a 16-bit ADC (LSB = 152.5 μV) would produce results of 2 and 17 (or 18) LSBs, for a ratio of 0.12 (or 0.11), an error of 10-20%. The relative error gets even worse for coarser resolutions. Thus the AD1330's operation makes possible accurate measurements of very small signals.

The second, a true-life example, comes from the field of medicine. Concentrations of some chemicals in a blood sample can be measured by observing changes in the sample's optical transmission—the ratio of the amount of light passing through the sample to that passing through a reference cell—over time, after treatment with a known amount of reagent (the ratio cancels out effects of variations in the light source). The concentration is then determined using the slope of a time-plot of these ratiometric results. Transmitted light can be very small for some chemistries.

Imagine that the transmitted signal is 267 μV. The AD1330 result is again 7 of the 38-μV LSBs (gain of 64). Suppose the reference signal is exactly 10,000 times bigger, or 2.670 V. The AD1330 processes a signal this large with unity gain (effective LSB = 2.44 mV) and the result is 1,094 LSBs. Each 2.44-mV LSB has the weight of 64 38-μV LSBs, so to find the ratio first multiply 1,094 by 64 (=70,016). The resulting ratio of 10,002.3 (= 70,016/7) is only 0.02% too large. A 0.05% gain error in the AD1330 (the maximum specification) would result in a reading of 1,095 2.44-mV LSBs, a ratio of 10,011.4 (0.11% error).

Compare this with the result obtained using an ideal conventional 16-bit ADC; it would measure 2 and 17,500 LSBs for the two voltages. The ratio of 8,750 (17,500/2) is *12.5% low*! An 18-bit ADC would be required to obtain accuracy comparable to that of the AD1330 for the ratio of these two very different signals. At this writing, no other known converter combines this level of resolution with the AD1330's 100-kHz throughput.

HOW DOES THE AD1330 WORK?

Block and timing diagrams (Figures 1 and 2) are helpful in understanding the AD1330's operation. Overall operation is shared by the two hybrid packages; the critical analog signal processing is performed in the Analog Input Section, while gain decisions, a/d conversion, data bus interface, and overall timing are handled by the Command and Control Section. This division of labors provides the lowest possible interaction between low-level analog signals and the high-speed digital data bus.

Here's what happens during one 10-μs AD1330 *Autogain* conversion cycle: First, the input signal is acquired by a low-noise track/hold (SHA #1) and the comparators determine the input's amplitude "window." Next, the control logic programs and enables the programmable gain amplifier (PGA) based on the comparators' outputs. Finally, an amplified version of the input is sampled and converted by SHA #2 and the 12-bit ADC. An analog feedback loop takes advantage of idle time in the conversion cycle to remove PGA offset. The relative timing of these events is shown in Figure 2. All internal operations are synchronized to the user-supplied 2.5-MHz clock.

The AD1330 signals the completion of each conversion cycle with an interrupt and makes available three 16-bit data words. Two words represent the conversion result and associated gain; by multiplying them the input signal can be reconstructed with 18 bits of dynamic range. The third word contains status flags indicating possible overrange conditions as well as the exact operating mode that produced the two data words.

Three primary operating modes are possible; they are selected using Write operations to AD1330 addresses. *Autogain* is described above. The AD1330's selection of optimum PGA gain during each conversion cycle is independent of previous cycles. Signal reconstruction requires two Read cycles per conversion, one for each data word. Autogain is the power-up default mode.

The two other operating modes are *Fixgain* and *Forcegain*. They permit I/O overhead reduction when *a priori* knowledge of the signal level is available. *Fixgain* has the effect of freezing the gain at the current setting. Subsequent conversions are performed at the "frozen" gain until the device is reprogrammed or reset. *Forcegain* allows the user to program the desired gain over the AD1330's data bus and keep it until another mode change is initiated. The AD1330's control logic ensures that mode changes are executed smoothly with no data loss or reduction in throughput. Fixgain and Forcegain are susceptible to overrange if the input exceeds the limits dictated by the chosen gain. This condition is flagged by a bit in the AD1330's status word.

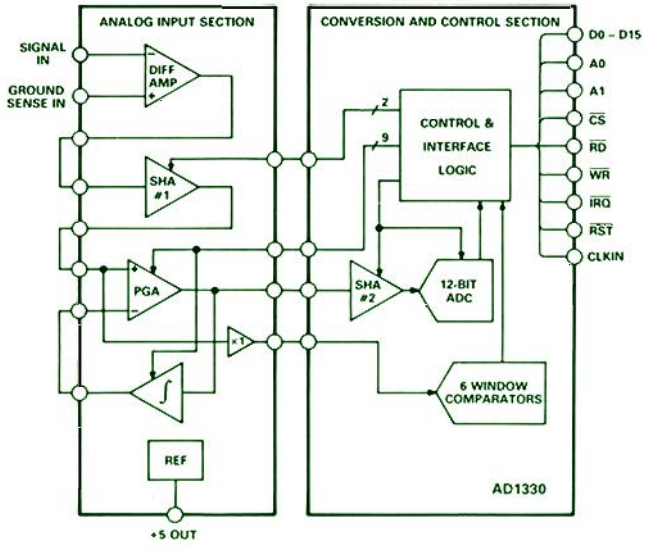


Figure 1. Functional block diagram of the AD1330.

A zeroing function, initiated by a Write operation, causes the AD1330 to measure and store any offsets present in SHA #2 and the ADC. The offset is digitally subtracted from all subsequent conversion results, preventing the introduction of spurious harmonic artifacts during signal reconstruction. This RTOCAL function (for Referred-To-Output CALibration) is performed automatically upon power-up and may be initiated at any time subject to the AD1330's overall timing constraints. Just one conversion cycle is required. The AD1330 stores its operating mode just prior to performing the single RTOCAL cycle and resumes operation in this mode when the calibration cycle ends.

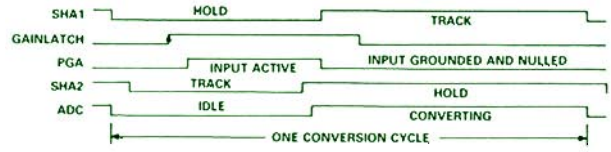


Figure 2. Simplified timing diagram.

The AD1330's high-speed data bus provides a direct, fully asynchronous interface to today's high-speed processors and requires no wait-state logic. The maximum data access and read cycle times are 15 and 25 ns over the full specified temperature range, increasing to only 25 and 35 ns for 100-pF loading.

SOME REAL-WORLD APPLICATIONS

The AD1330 has generated broad interest. Commercial applications include colorimetry, chromatography, mass spectrometry, spectroscopy, and other analytical contexts. In all these cases the information is often used ratiometrically, although the absolute signal levels can range from microvolts to volts. The wide dynamic range of the AD1330 ideally suits these criteria.

Another general area of commercial interest is *vibration analysis*, where signals can have a wide range of amplitudes and frequencies. An example is data acquisition systems for automotive crash-testing. Many governments require verification of model crash-worthiness. Considerable money could be saved by reducing the number of test vehicles if the amount of data acquired per vehicle were increased, but the space and power available for the instrumentation package are limited. The AD1330 makes it possible to increase the number of signal channels per vehicle while satisfying these constraints.

Military applications abound. One area of interest is *digital radio* sets, where the AD1330 can be used to replace conventional AGC circuits. Their fast attack and slow decay is susceptible to certain jamming strategies. The AD1330's 10-μs response to signal changes provides a means of improving jam-resistance. In *sonar signal processing*, signal amplitudes can vary widely with the size and position of the target. The AD1330 is well-suited to handling these conditions and is fast enough to handle many sensor channels multiplexed through a single converter system.

WHAT'S AVAILABLE?

The AD1330KD is available now for operation over the 0 to +70°C temperature range; a fully qualified /883 version for −55 to +125°C will be available soon. Prices start at $310 (100s).

DISTRIBUTED DATA ACQUISITION AND CONTROL WITH FLEXIBILITY

μMAC-1050 Offers Variety of Analog and Digital I/O Options

On-Board Microprocessor Handles Scaling, Alarms, Serial Ports

by Tom Kelly and Raouf Bortcosh

The μMAC-1050* is a complete, low-cost, distributed subsystem for data acquisition and control in applications such as chemical or biological pilot plants, HVAC (heating/ventilation/air conditioning), and energy-management systems. The basic building block is a 7"x 9" circuit board that integrates analog I/O, digital I/O, microprocessor, memory, and a serial communications port with operating-system firmware.

A host computer (e.g., a standard PC) communicates with the μMAC-1050 in a command/response format to implement a powerful instruction set for I/O-related functions and internal operations. With it the user can configure channels, set alarm limits, read analog and digital I/O values, set up the electronic cam sequencer, configure the special pulse I/O and event counting inputs—and check status and alarm registers.

The system firmware for the μMAC-1050 is stored in PROM and is available immediately on power-up. This firmware includes an analog and digital I/O scanner, communications driver, numerical routines, self-test, and field calibration. The user sets I/O configuration data and stores it in on-board EEPROM; this prevents it from being lost if power is lost or disconnected.

The basic μMAC-1050 circuit board (Figure 1) uses an 80C188 16-bit CPU running at 8 MHz. Memory consists of a 32K PROM, an 8K-RAM workspace, and a 2K electrically erasable ROM for storing data provided by our factory as well as user configuration data. To allow communication at 38.4 kilobaud, a UART interfaces to the CPU with direct memory access (DMA). Analog outputs are electronically adjusted; this avoids problems with trim potentiometers and facilitates recalibration. A watchdog timer monitors circuit operation and activates an alarm output if it determines that a major malfunction of the system has occurred.

Analog I/O: A single μMAC-1050 can acquire 48 channels of analog input via its 16 (single-ended) channels of on-board input and up to 32 more channels via analog expansion panels. A 14-bit

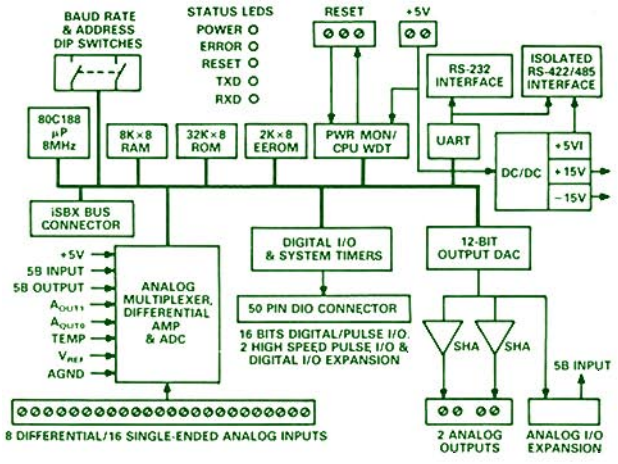
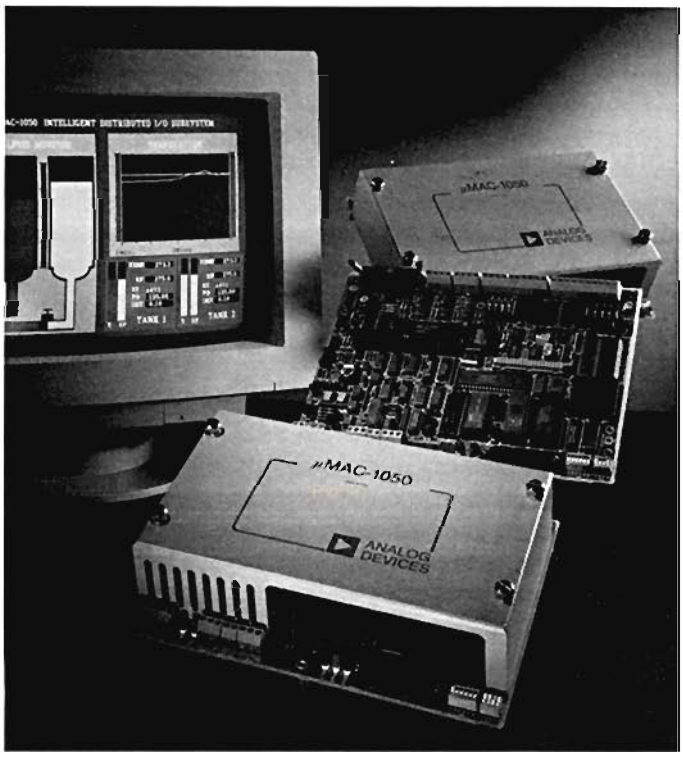


Figure 1. Block diagram of the μMAC-1050.

*Use the reply card or call 1-800-4-ANALOG for technical data.



(plus sign) integrating a/d converter (16.67-ms conversion time at 60 Hz, 20-ms at 50 Hz) provides high-accuracy (better than ±0.005% of span) combined with 90 dB of common-mode rejection. Each channel's input mode can be configured independently in software for single-ended or differential connections, maximizing available channels while maintaining signal-conditioning requirements. The μMAC-1050 also supports six auxiliary input channels; two are for measuring base unit temperature and +5-V supply voltage; the other four service cold-junction-compensation sensors on expansion panels when thermocouples are used.

Additional common-mode rejection is provided when using signal-conditioning modules in the Analog Devices 5B Series for millivolt- and volt-level signals, as well as thermocouples, RTDs, and strain gages; they also provide input-output isolation (1,500 V rms) and overvoltage protection (240 V).

Expansion panels with 8 or 16 channels increase the number and type of served channels beyond the capabilities of the basic μMAC-1050. Specialized panels are available for low-level signals, such as thermocouples, which require isolation; for high-level 5- and 10-volt signals; and in non-isolated versions. Analog I/O panels can be mixed as needed (Figure 2).

For analog output, two ±10-volt on-board channels can be supplemented by eight additional channels on expansion panels, all with 12-bit resolution. Expansion panel ranges for output include 0-5 V, ±5 V, 0-to-10 V, ±10 V, 0-to-20 mA, and 4-to-20 mA. Outputs can be programmed to come up at a desired value upon power-up, and to ramp when changing values. Output readback is available to check the output setting.

In operation, the user characterizes and identifies each input and output channel type through software. As each channel is configured it is entered into the *scan list* of channels to be continuously scanned. For inputs, the a/d converter performs digitizing, and the microprocessor of the μMAC-1050 performs linearization, scaling, and alarm checking. The a/d conversion function is automatically recalibrated against an internal reference voltage and analog ground once per scan to eliminate most of the analog-circuit drifts that can affect long-term accuracy.

Digital I/O: A digital I/O connector provides access to the sixteen TTL-compatible on/off I/O lines of the base μMAC-1050 unit. Each digital point is configurable as input or output, and they can be arranged in any mix of time-proportional pulse output, pulse- and period measurement, and pulse counting. The base unit's sixteen channels can be increased to 64 channels with expansion panels which "daisy-chain" to the main panel.

The sixteen digital I/O points can be used independently; eight of them can also be joined to emulate a motor-driven cam sequencer of up to 128 steps. In this mode, a table is set up in software (and stored in EEPROM); it defines the state of the eight outputs and specifies how long this state should be maintained (in 10-ms increments). After the table is executed, it can stop or repeat; the table can also be entered at any step—or incremented one step at a time—by software command.

Many applications require digital pulse I/O optimized for high-speed digital signals. To meet this need, the μMAC-1050 provides two channels of high-speed pulse I/O (up to 1-MHz operation) for event counting and time-proportional output as might be needed to drive electric heating elements which control the average heat level by modulating the pulse duty cycle.

Command Set: The command set is used to configure I/O, access I/O channels, establish control, and read status. Its six main groupings are analog input, analog output, digital I/O, cam sequencer, pulse I/O, and status & control.

Processing: To maintain system integrity despite link- or host failure, the μMAC-1050 can implement alarm-related actions on critical points, in addition to reporting out-of-bounds inputs to the host in response to queries (Figure 3). As many as 32 of the analog input channels can have four levels of alarm; each alarm can control the state of a digital output.

Limit-checking and alarm-setting are done entirely within the μMAC-1050, *independently of the host*, and will function even if the host is unavailable. To give the user additional flexibility, the alarm output can be configured to either *latch* on alarm, where it must be reset by the host, or automatically return to its initial state when the out-of-limit condition ceases.

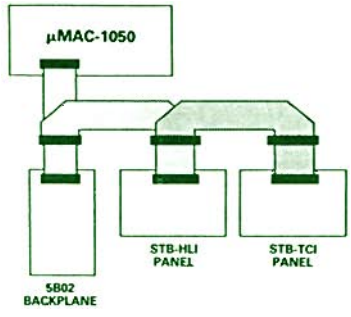


Figure 2. Daisy-chaining multiple analog I/O panels from a single μMAC-1050.

The μMAC-1050 can also store and report, on demand, the maximum and minimum values of analog inputs. Available for all channels, this eliminates the need for perpetual queries (and consequent excessive communications activity) just to see if a new maximum or minimum has occurred. All analog values are stored and manipulated as real numbers (IEEE short floating-point format) for a more-accurate and "host-friendly" data format.

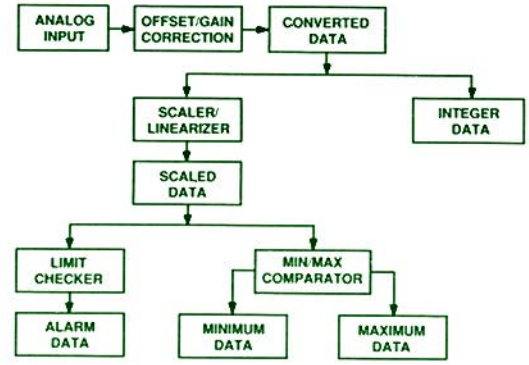


Figure 3. Processing of analog inputs.

Protocol and Communications: All communication between the host and μMAC-1050 is over a serial link operating at up to 38.4 kilobits per second. Numerical values are returned as 4-byte floating-point numbers using IEEE standard format, or as integer values from −16384 to +16383. The latter format requires only half as many data bytes to be transmitted, but processing at the host is needed for it to be fully useful.

The user can request an analog value from a single channel or a scan across a group of channels. At 38.4 kbps, the effective rate—from initiating a request to getting the last data byte from 48 channels, using integer format—is 1,411 channels/second (vs. 728 channels/second using real-number format). The time for a single-channel integer reading, from request to response, is 5.6 ms; the corresponding real-number-format value is 8.8 ms.

The μMAC-1050 is connected to the host using either an RS-232 port or an RS-422/485 port (available at separate connectors). As many as 64 μMAC-1050s can be multidropped over one serial link to the host using the RS-422/485 port, at a maximum overall distance of 5,000 feet. This port is optically isolated for optimum performance in noisy environments.

Applications Software: To enhance the ease-of-use of the μMAC-1050, a profusion of applications software is available, including DOS Drivers for many standard PC languages. An *I/O Commander* is shipped with every unit to permit quick set-up and exercise.

Industry-standard menu-driven software packages that run the μMAC-1050, and display and analyze results after simple user setup, include: THE FIX and FIX DMACS from Intellution, LABTECH NOTEBOOK and LABTECH CONTROL from Laboratory Technologies, and Control EG from Quinn-Curtis. These software packages, available through Analog Devices, require only setup and configuration specific to the μMAC-1050 hardware and the needs of the application.

The μMAC-1050 arrives ready to hook up to your power supply and host cable. The basic small-quantity price for μMAC-1050 is $995; a comprehensive instruction manual and numerous accessories are optional and priced separately.

HIGH-PERFORMANCE ELECTROMETER OP AMP IN 8-PIN PLASTIC DIP

AD546K Has < 0.5-pA Bias Current, < 1-mV Offset, 20 μV/°C Drift, Autoinsertable Packaging; Low Cost for Photodiode Arrays

The AD546* electrometer-type op amp is a precision device with bias currents below 1 pA housed in a cost-effective 8-pin plastic mini-DIP package. The AD546J/K feature subpicoampere bias current (1/0.5 pA max at room ambient temperature), laser-trimmed input offset voltage (2/1 mV max), and low input offset voltage drift (20 μV/°C). Maximum input bias current is 100% tested and guaranteed in a fully warmed-up configuration. Price is low, only $3.75/$4.50 in 100s.

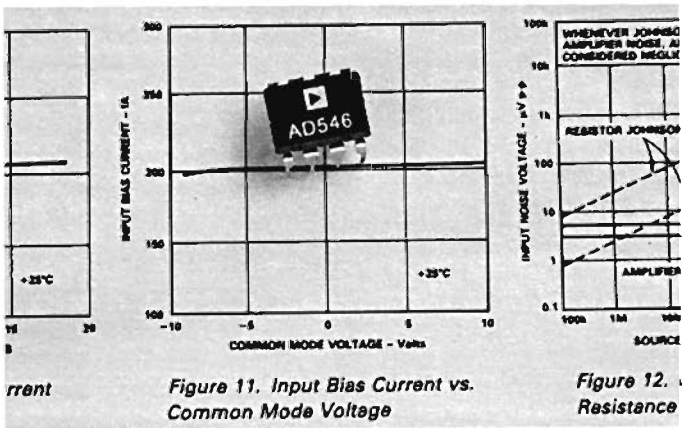
High-impedance, weak current sources such as photodiodes, ion-selective electrodes, pH probes, and X-ray detectors require amplifiers with extremely high impedance to minimize loading in the voltage mode (noninverting buffer amplifier) and low bias current to minimize error in the current mode (voltage-to-current converter or integrator. Chromatographs, spectrometers, and medical and scientific instrumentation are typical applications for these sensors. Many new-equipment designs using an array of sensors instead of the one or two sensors of earlier designs benefit from lower-cost, autoinsertable electrometer op amps.

Such amplifiers are typically applied as current-to-voltage converters measuring extremely low input currents. Due to the high impedances and extremely small curents, the op amp must be applied carefully both electrically and mechanically. Plastic packaging has heretofore been regarded as unacceptable for consistent performance, but the AD546 in its plastic package has demonstrated proven reliability in storage tests at high temperatures and humidities.

The AD546, like the proven AD549 (*Analog Dialogue* 21-2, 1987) is based on patented "topgate" JFET technology. The bootstrapped input stage design results in 10^{15}-Ω common-mode impedance, with input bias current essentially independent of common-mode voltage. AC performance includes 3-V/μs slew rate and 1-MHz unity-gain bandwidth. Voltage noise, often critical in electrometer applications, is 4 μV peak-to-peak from 0.1 to 10 Hz; current noise is 1.4 fA p-p over the same frequency range and is thus negligible in most applications.

Thermal Effects: From its room-temperature value, the bias current of the AD546 will increase by a factor of 2.3 per 10°C temperature rise, (characteristic of all JFET-input amplifiers). On-chip dissipation raises chip operating temperature, causing increased bias current. But the AD546's low quiescent supply current (700 μA for ±15-V supplies) causes junction temperature to increase just 3°C above ambient. However, heavy output loads will cause dissipation, chip temperature, and—consequently—bias current to increase significantly. Therefore, minimum load resistance of 10 kΩ is recommended; however, when necessary, an AD546 can safely provide at least 15 mA into a short-circuit load. The amplifier is stable at gain of +1 with a 4,000-pF capacitive load.

Maintaining Performance on Boards: The finite (leakage) resistance between the input terminals and adjacent pins on the IC



rrent — Figure 11. Input Bias Current vs. Common Mode Voltage — Figure 12. Resistance

package—and between the input leads and adjacent traces on a circuit board—causes errors: the voltage differences produce parasitic currents in the signal paths of both inputs, developing output error. For example, 10,000 MΩ between the + input and the adjacent −15-V supply pin would allow 1.5 nA (1,500 pA) to flow—much more than the 1-pA bias-current spec.

Leakage is minimized by maintaining high insulation resistance and guarding input lines to the AD546. Boards must be kept clean, dry, and free of contaminants, such as solder flux, via proper cleaning procedures and bake-drying. Guard traces on both top and bottom of the circuit board and alongside the input trace, when connected to ground (for inverting operation) or the R_F-R_I junction (for follower configuration with a low-resistance feedback divider), minimize leakage via low *surface* resistance.

To overcome limited circuit-board *volume* resistivity, especially in high humidity conditions, the input pin of the AD546 can be (carefully) bent up and soldered directly to a Teflon-insulated standoff. The input signal and feedback component leads must also be insulated and rigidly mounted by standoffs and/or low-leakage guarded and shielded cable to avoid vibration-induced interference.

The AD546J &K grades, specified for 0 to +70°C operation, have 1.0 & 0.5-pA bias current.

The AD546 was designed by JoAnn Close of Analog Devices Semiconductor Division, Wilmington, Mass.

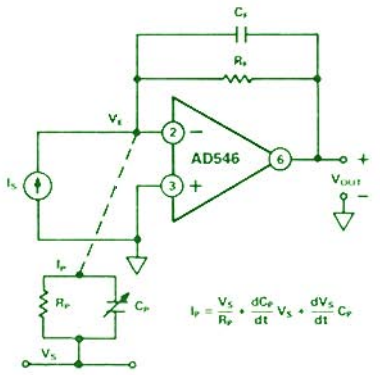


Figure 1. Sources of parasitic leakage current.

*Use the reply card for technical data.

INDUSTRY'S FASTEST MONOLITHIC FET-INPUT OP AMP

AD843 Slews at 250 V/μs with 34-MHz Unity-Gain Bandwidth Settles to 0.01% IN 135 ns; Has only 1 nA Max I_b, 1 mV Max V_{os}

by Robert M. Clarke

The industry's fastest monolithic FET-input op amp, the AD843,* slews at 250 V/μs and has a 34-MHz unity-gain bandwidth. Not sacrificing precision for speed, the amp features a paltry 120-pA input bias current but quickly settles to within 0.01% in 130 ns for a 10-volt step (Figure 1). A member of the AD84X family* of high-speed operational amplifiers (see *Analog Dialogue* 22-2, 1988, pp. 12-15), the AD843 is fabricated using Analog Devices' junction-isolated complementary-bipolar (CB) process. This process permits a combination of dc precision and wideband ac performance previously unattainable in a monolithic FET-input op amp.

The AD843 serves in high-speed applications that previously required discrete or such hybrid FET-input amplifiers as the ADLH0032, combining such features as low input bias current, fast slew rates, fast settling time, and large unity-gain-bandwidth products. The AD843 is the first monolithic FET-input op amp to fulfill these needs. Prime applications for the AD843 include high-speed sample-holds, peak detectors, high-speed integrators, active filters, and fast current-to-voltage (I/V) converters. The 250-V/μs slew rate and 120-pA typical input bias current of the AD843 ensure excellent performance in high-speed sample-hold circuits and high-speed integrators, where low input-bias currents minimize circuit errors, while high slew rates and fast settling times allow the amplifier to track the input signal accurately. This amplifier is also ideally suited for high-bandwidth active filters and high-frequency signal-conditioning circuits.

The AD843's 1.0-nA (K/B grades) or 2.5-nA (J/A/S grades) maximum input bias current *fully warmed up at room ambient*, and maximum of 23 nA over temperature (K grade), differentiate it from other Analog Devices high-speed op amps. An op amp's input bias current is a critical specification for sample-hold amplifiers (low bias current equals low droop) or in any other circuit in which charge is stored in a capacitor (e.g., peak detectors and AGC rectifiers). Also, low input bias current means lower dc-offset errors when the amplifier is used high-input-impedance filters, integrators, or I/V converters.

Figure 2 shows a peak-detector circuit that can accurately track increasing waveforms, capture the amplitude of an input pulse as

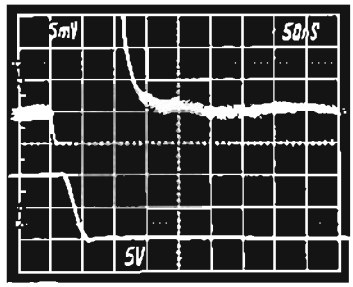
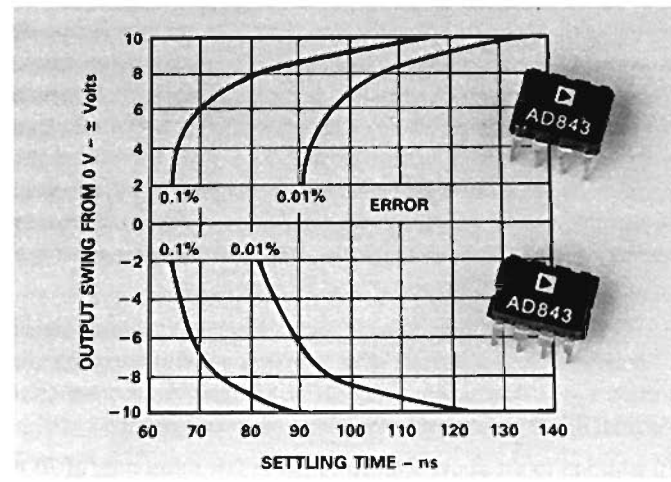


Figure 1. Final settling of the AD843 for a +10-volt-to-zero step change. Upper trace: amplified (×10) error voltage (0.01% per division). Lower trace: AD843 output.

*Use the reply card for technical data.



narrow as 200 ns, and hold it with a droop rate of less than 20 μV/μs. As shown, it will capture peaks of positive waveforms; with reversed diode polarity, it will follow decreasing waveforms and hold negative peak values. The AD847* input amplifier (another member of the fast AD84X monolithic op-amp family) can drive the 680-pF Hold capacitor fast enough to catch a peak in 100 ns and settle to the new value in 250 ns. Smaller capacitance values increase speed at the expense of increased overshoot and droop; larger capacitance values (driven stably by the AD847) decrease droop at the expense of response time.

Unlike many high-frequency amplifiers, the AD843 requires no external compensation for gains ≥ 1. It remains stable over its full operating temperature range. The AD843 also offers low quiescent current (13 mA max), high output-current drive capability (50 mA minimum at ±10 V), low noise (19 nV/√Hz), and low input offset voltage (1 mV max—K and B grades).

It is available in two performance grades apiece for operation at 0 to +70°C (J,K) and –40 to +85°C (A,B); and a military "S" grade is available (with /883 processing option) for –55 to +125°C. Packaging is available in 8-pin plastic mini-DIPs, cerdip, and 12-pin hermetic metal cans. Prices start at $8.80 (100s).

The AD843 was designed by Wyn Palmer at Analog Devices Semiconductor Division, Wilmington, Massachusetts.

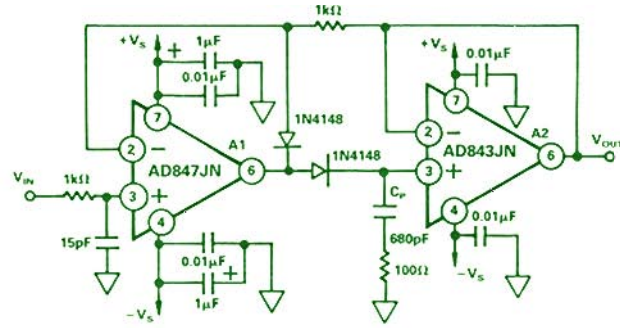


Figure 2. Fast peak-detector circuit.

COMPLETE MONOLITHIC 12-BIT DAC INTERFACES WITH FAST DSPs

AD7848 Has 8-Word FIFO for Independent Loading and DAC Update

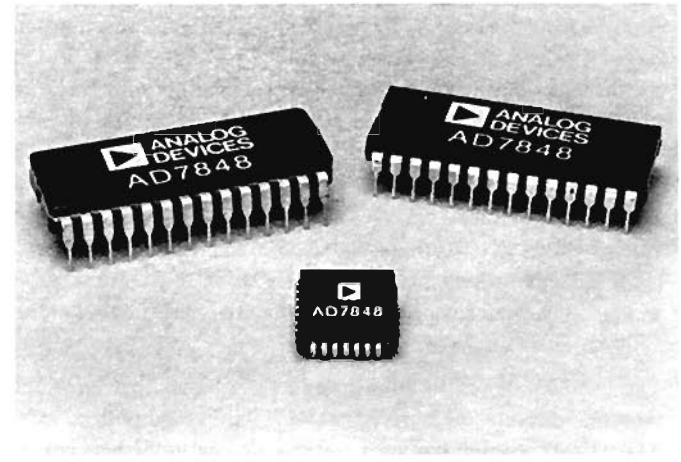
Requires 42-ns Minimum $\overline{WR}$ Pulse, Has 70-dB SNR for 10-kHz output

The AD7848* is a fast, complete, 12-bit voltage-output d/a converter with a versatile interface to digital signal processors. Its conversion circuit contains (Figure 1) a precision 3-volt buried Zener reference and an output buffer amplifier with 4-μs settling time. Its interfacing circuitry includes an 8-word × 12-bit first-in-first-out (FIFO) memory and associated control logic. The FIFO allows data to be captured whenever the processor makes it available at full microprocessor speed; the DAC register (and hence the analog output) is subsequently updated asynchronously as required by the analog portion of the system.

The AD7848 is fully specified for ac parameters, including signal-to-noise—SNR (70 dB max over temperature) and harmonic distortion (–80 dB typical), with ±1/2-LSB relative accuracy (K,B versions). It is guaranteed monotonic over temperature.

In addition to the above features, it has a fast setup time of 20 ns and write pulse width of 42 ns; this allows it to interface directly with DSP processors and high-speed 16-bit microprocessors. Typical applications are in speech synthesis, high-speed modems, adaptive noise cancellation, and as an analog output port for digital signal-processing (as such, it is useful in DSP-controlled real-time function generation). It can be teamed (Figure 2) with a FIFO ADC, such as the AD7878 (*Analog Dialogue* 22-2, page 21), in digitally processed servo-control systems.

Eliminating the interrupt: In a real-time system application, where analog data is acquired and processed—resulting in data which must be returned to analog form at a real-world sampling rate—the processor (unless dedicated) would have to service an interrupt periodically. That requires software overhead, and places unnecessary demands on a hard-working digital signal processor, which has the paramount task of computation. The FIFO buffer, which acts as a "time buffer" between the DSP's machine time and the real-time sample rate, can eliminate this problem, since DSP results can be placed on the bus as they occur in (aperiodic) machine time, and the DAC register (hence the output) can be updated periodically in real time.



The AD7848 has a 3-volt reference and a bipolar output range of ±3 volts, which responds to twos-complement-coded digital input. Two grades each are available for 0 to +70°C (J,K—in plastic DIP or PLCC) and –40 to +85°C (A,B—in hermetic DIP); they differ only in SNR for 1-kHz sine wave sampled at 100 kSPS (72 dB min for K,B, 70 dB min for J,A) and relative accuracy (±1/2 LSB for K,B, ±1 LSB for J,A). An "S" grade is available for –55 to +125°C, packaged in a hermetic DIP. Prices start at $9.85 (100s) for the "J" versions.

The AD7848 was designed by P. J. Garavan at Analog Devices, BV, in Limerick, Ireland.

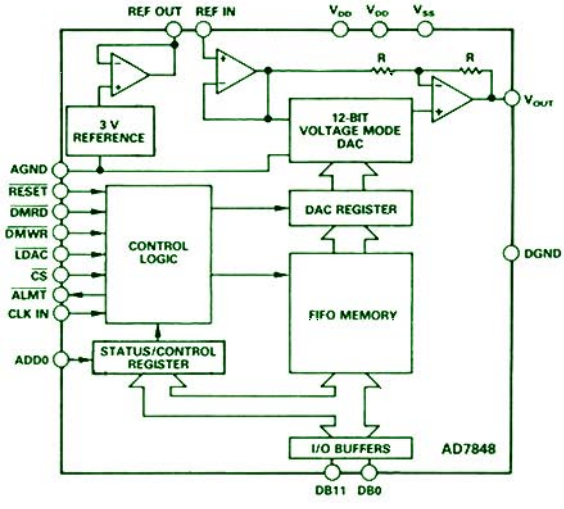


Figure 1. AD7848 block diagram.

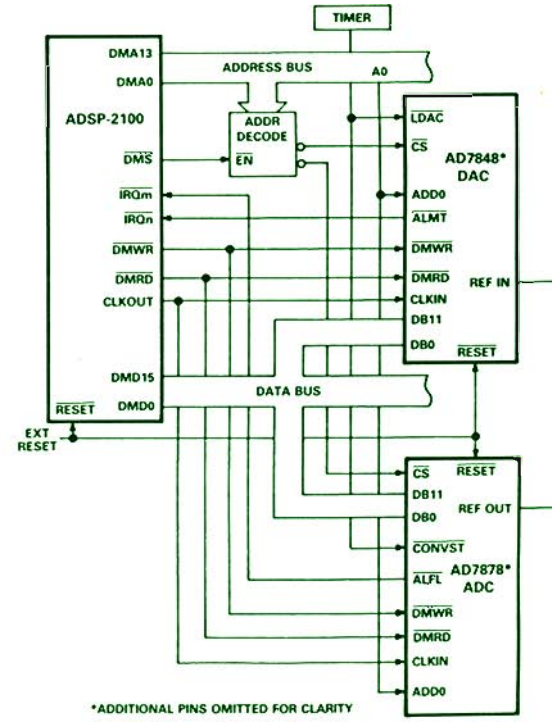


Figure 2. Interfacing the AD7848 DAC and an AD7878 ADC with the ADSP-2100 DSP microprocessor.

*Use the reply card for technical data.

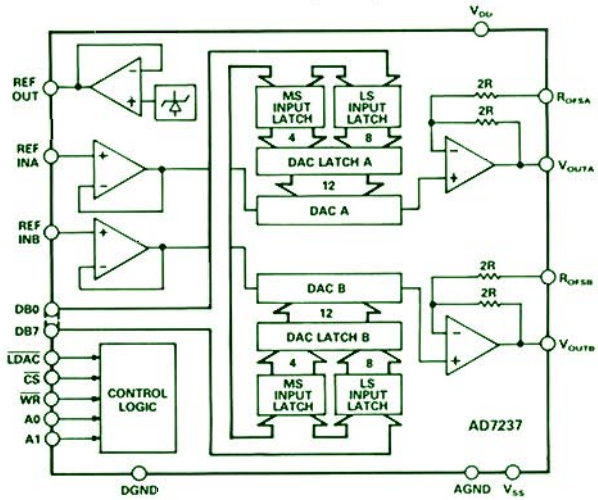
MONOLITHIC DUAL 12-BIT DACPORTS SAVE SPACE, POWER, COST

Complete in PLCC or 0.3" DIP with Reference and Output Amplifier

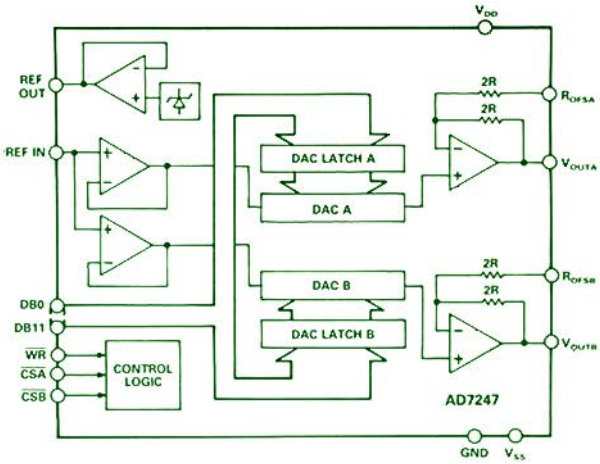
AD7237 Loads 8-Bit Bytes; AD7247 for 12-Bit Parallel

The AD7237 and AD7247* are complete dual 12-bit voltage-output digital-to-analog converters (DACs) on monolithic CMOS chips, packaged in 28-terminal PLCCs or 24-pin "skinny" 0.3"-wide plastic or hermetic ceramic DIPs. They include output amplifiers and a buried-Zener laser-trimmed 5-volt reference and are microprocessor-compatible, with interface logic and high-speed data latches. Full specified linearity (i.e., ±1/2 LSB max relative accuracy error over temperature—K,B,T grades) is achieved without calibration cycles or external user trims.

These compact DACPORTs™ differ (Figure 1) only in the type of data bus each interfaces with. The **AD7247** accepts 12-bit parallel data, which is loaded into the selected DAC latch using the $\overline{WR}$ input and a separate Chip Select input for each DAC. The **AD7237** has a double-buffered interface structure and an 8-bit-wide data bus; two bytes of data are loaded to the respective input latch in two Write operations; then an asynchronous $\overline{LDAC}$ signal updates the DAC latches and analog outputs.



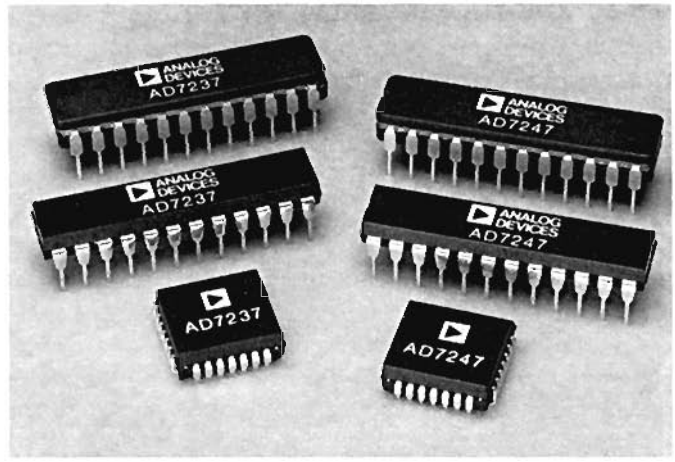
a. AD7237 loads from 8-bit bus in two Write operations.



b. AD7247 accepts 12-bit parallel data.

Figure 1. Functional block diagrams.

*Use the reply card for technical data. DACPORT is a trademark of Analog Devices, Inc.



Their compact architecture and packaging make them useful wherever multiple general-purpose 12-bit DACs are required to conform with constraints of space, power (only 300 mW with ±15-volt supplies, 165 mW in +15-volt single-supply operation), and cost. In addition, their typical ±1-LSB mismatch of full-scale error makes them useful in applications calling for pairs of matched DACs that track over temperature. Prices are identical for both types. They begin at only $15.00 (100s).

The AD7237 and AD7247 will interface with both general-purpose and DSP microprocessors. Figure 2 shows the AD7247 interfacing with an ADSP-2101 digital signal processor. The 12-bit word is written to the selected DAC latch of the AD7247 in a single instruction, and the analog output responds immediately. Depending on the ADSP-2101's clock frequency, only one or two programmed wait states will be necessary.

Guaranteed monotonic, these devices are available in two grades (J,K; A,B; S,T), differing only in relative accuracy (±1 LSB, ±1/2 LSB) for each of the three popular temperature ranges (0 to +70°C; –40 to +85°C; and –55 to ±125°C). Pin-jumpered output-voltage ranges are 0 to +5 V, 0 to +10 V, and ±5 V. ±Full-scale-output settling time is 10 µs max on the +5 and ±5-volt ranges.

The AD7237 and AD7247 were designed by Conor McAuliffe at Analog Devices, BV, in Limerick, Ireland.

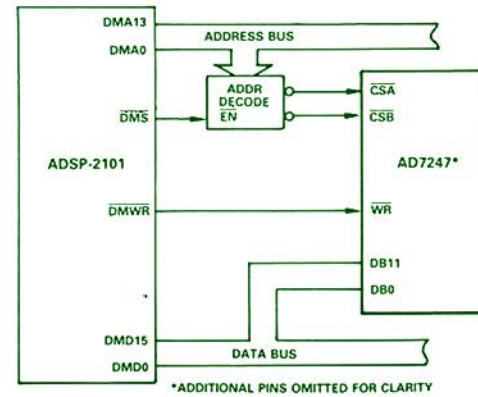


Figure 2. Interfacing the AD7247 to the ADSP2101 DSP.

FAST PRECISE COMPARATOR HAS WIDE DIFFERENTIAL INPUT RANGE

AD790 Has Min/Max Specs for Both ±15-Volt and +5-Volt Operation

Propagation Delay is 45 ns Max (±15 V), 50 ns Max (+5 V)

The AD790* is a versatile, fast, precise voltage comparator on a single monolithic chip (Figure 1) fabricated in the Analog Devices complementary-bipolar (CB) process, discussed recently in these pages (22-2, 1988, pp. 12-15). It operates on a wide range of supply voltages and is fully specified for performance under two conditions: with a single +5-V supply and with dual ±15-V supplies. It will accept differential input voltages up to $\pm V_S$, and its outputs are compatible with both TTL and CMOS levels.

The output of a comparator, like that of an open-loop high-gain op amp, attains one of two output levels to represent the polarity of the difference between its two inputs. But as the difference passes through zero, even small amounts of noise can cause a comparator's output to rattle back and forth. To combat this universal tendency, the AD790 has an internal positive-feedback circuit, which provides typically 1/2-millivolt of hysteresis to reduce sensitivity to noise while maintaining high resolution.

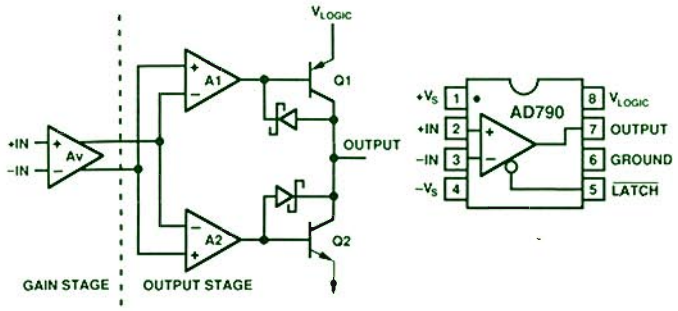


Figure 1. Block diagram and connection diagram (8-pin plastic mini-DIP and Cerdip).

With ±15-volt supplies, the 0-to-70°C J/K grades of the AD790 have a maximum 45-ns propagation delay (over temperature) with a 100-millivolt step and 5-mV overdrive; the propagation delay increases to 50 ns max for the –40 to +85°C A/B grades and to only 60 ns max for the –55°C to +125°C "S" grade (also available to /883B). In +5-volt operation, these numbers increase to 50, 60, and 65 ns maximum. Typical variation of propagation delay with overdrive and temperature is shown in Figure 2.

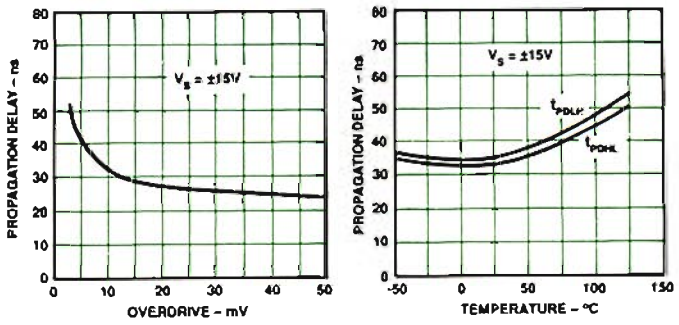
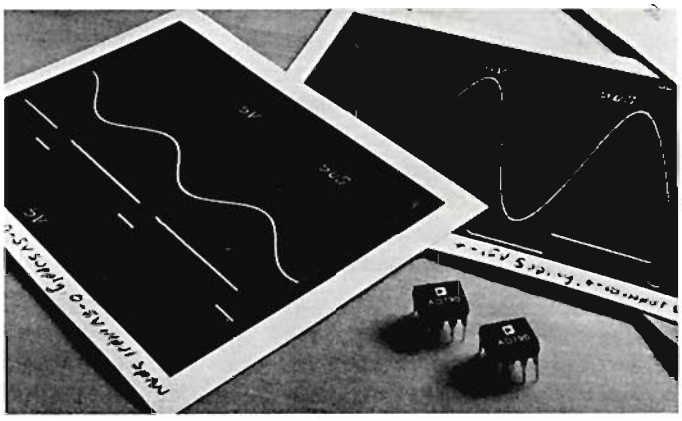


Figure 2. Propagation delay vs. overdrive and temperature.

*Use the reply card for technical data.



With ±15-volt supplies, the K and B grades have 0.5-mV max offset, 4.5-μA max bias current, and 85-dB min CMR and PSR over temperature, dissipating 242 mW max. +5-volt Operation with +5-volt supplies degrades the specs slightly; but dissipation drops to 60 mW. Prices start at $2.95 in 100s.

Applications: Because of its speed, stability, and ability to resolve differences of less than 1 millivolt, the AD790 is useful in a wide variety of applications, including zero-crossing detectors, pulse-width modulators, and precision rectifiers. Its wide range of differential input makes it useful in overvoltage detectors. Since it is, in effect a 1-bit a/d converter, it is helpful in building user-designed a/d converters, including delta-sigma types.

As an example of its applications, Figure 3 shows a single-supply *overcurrent detector* circuit for a grounded load, in which the current is measured by a voltage developed across a low-value resistor formed by a segment of printed-circuit-board trace; the voltage is then compared with a reference (trip) voltage of 10 mV, established by the comparator's minus-supply current through a 2.7-ohm resistor.

The AD790 was designed by Chris O'Connor at Analog Devices Semiconductor, Wilmington MA.

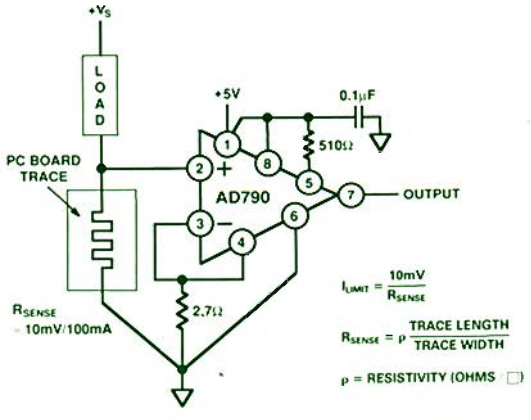


Figure 3. Overload-detector application.

ULTRAFAST MONOLITHIC SINGLE & DUAL TTL COMPARATORS

AD9696 & AD9698 Have 4.5-ns Propagation Delay, 100-ps Dispersion Work on +5 or ±5-Volt Supplies, Have Complementary TTL Outputs

The AD9696 and AD9698* are ultrafast TTL-compatible differential voltage comparators that can achieve propagation delays previously possible only in high-performance ECL devices. They compare two input signals and provide a TTL output that depends on the polarity of the difference between the input signal levels. With ±5-volt supplies (actually +5, −5.2 V), they have typical propagation delay of 4.5 ns (7.0 ns max) over temperature, for a 100-mV pulse with 20-mV overdrive. Propagation delay dispersion is typically 100 ps (200 ps max) for overdrive from 50 mV to 1.0 V; and setup time is only 1.7 ns (Figure 1).

Besides offering a speed improvement, these comparators also have excellent accuracy specifications: 3 mV maximum offset voltage over temperature (all grades), 70 µA maximum bias current over temperature, and 1.3 µA max *offset* current over temperature.

Both devices operate on +5-volt or ±5-volt supplies. With a +5-volt supply, the common-mode input range over the full temperature range is +1.4 V to +3.7 V; with a dual supply, the lower end of the range becomes −2.2 volts. Common-mode rejection over temperature is 80 dB min with dual supplies, 57 dB min with a single +5-volt supply.

There are two grades of both devices, K and T, with identical performance specifications, except for temperature range: 0 to +70°C and −55 to +125°C. All devices are available in Cerdip; the 0 to +70°C AD9696K and AD9698K are also available in a plastic DIP and SOIC; and the single comparators, AD9696K/T, are also available in the TO-100 can. Prices (100s) start at $3.50/$6.00 (AD9696KN/AD9698KN).

Applications: High-speed comparators are widely used in data communications and test equipment, as well as computers, instrumentation, radar/sonar, and imaging. The AD9696 and AD9698 can be used in many cases to provide a pin-compatible (in DIPs) speed upgrade for slower competitive devices and the AD9686.

Figure 2 shows a window comparator circuit using the AD9698; it combines speed, TTL compatibility, and ease of application.

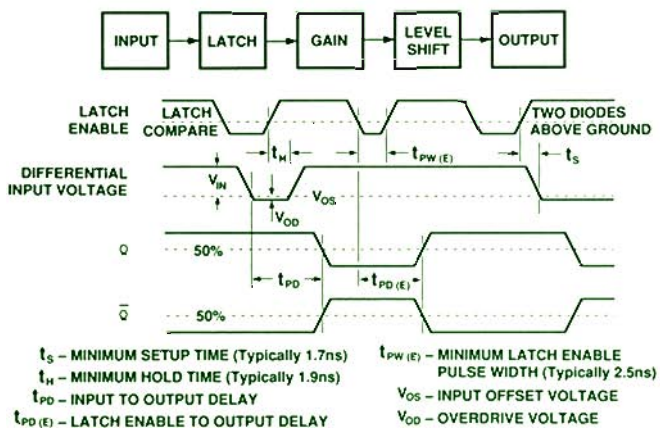
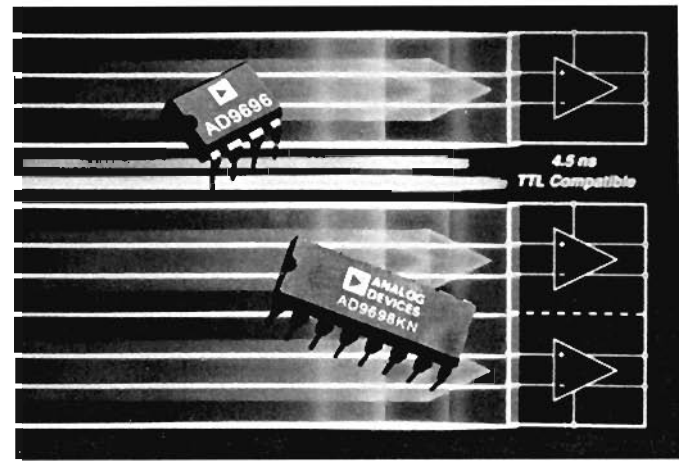


Figure 1. Architecture and timing diagram.

*Use the reply card for technical data.



Window comparators are used to determine when a signal's voltage level is within (or outside) a particular voltage range.

To establish a "window" with upper and lower voltage thresholds, two comparators are required. For such an application, the dual comparator saves space and cost; in addition, the two-comparators-on-a-chip design provides a degree of matching of dc and time-skew characteristics.

The window is formed by providing the desired $+V_{REF}$ to the noninverting input of the upper comparator and the lower limit, $-V_{REF}$, to the inverting input of the lower comparator. The input signal is connected to the remaining input terminals. The limit voltages can be any values in the specified input range (so long as $+V_{REF} > -V_{REF}$); for example, when ±5-volt supplies are used, acceptable pairs would include +2.0 V, +1.0 V; −1.0 V, −2.0 V; +2.0 V,−2.0 V.

The truth table for the comparator is:

$V_{SIGNAL} > +V_{REF}$	$Q_1 = 0, Q_2 = 1$
$-V_{REF} < V_{SIGNAL} < +V_{REF}$	$Q_1 = 1, Q_2 = 1$
$-V_{REF} > V_{SIGNAL}$	$Q_1 = 1, Q_2 = 0$

When the signal is in the window, the output of the AND gate goes high. It is low for all other conditions. An OR gate with the $\overline{Q1}$, $\overline{Q2}$ outputs would establish a complementary window.

The AD9696 and AD9698 were designed by Perry Jordan, at Computer Labs Division of Analog Devices, Greensboro, NC.

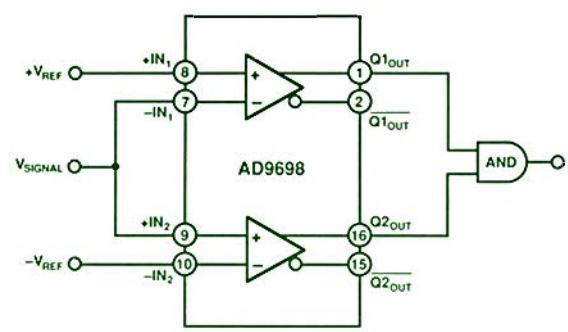
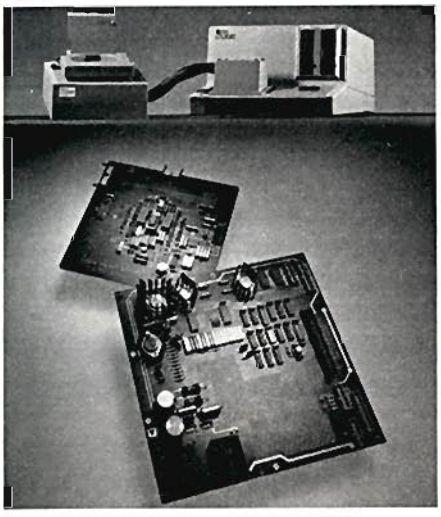


Figure 2. AD9698 as a window detector.

PWM TEST BOARDS

Enhance Mixed-Signal Bench Test System



Since 1984, the LTS-2020 Component Test System.* has grown to provide menu-driven, BASIC-programmable testing of linear, digital, data-conversion, discrete, and recently, mixed-signal devices (23-2, pp. 16-17). Now it also does ac and dc parametric tests on pulsewidth modulators,* via the LTS-0401 PWM Expansion Board, LTS-0382 General-Purpose Performance Board—to test a wide range of PWMs, and the specialized LTS-0381 1524 Performance Board—to test 1524-Series PWMs.

The *LTS-0401* has: a multi-range V/I source of up to ±110 V for inputs and for output leakage tests; a 16-bit frequency counter for measuring oscillator frequency and testing duty cycle; and space (20 in²) for additional user-designed circuitry for specialized applications.

The *LTS-0382*'s op-amp loop has adjustable common-mode voltage to test dc parameters and a fast ±peak detector for oscillator-amplitude and ramp-voltage tests. A switchable high-speed buffer facilitates measuring frequency, pulsewidth, and other ac parameters. On-board circuits can access a variety of signals and other resources, and an uncommitted area is for user circuitry. The board is configured by connecting resources to appropriate DUT pins. The similar *LTS-0381* tests 1524/2524/3524-series PWMs; it includes documentation and software. Price for each board: $1,900.

*Phone Analog Devices Component Test Systems for information: 1-508-658-9400.

FAST PRECISION FET-INPUT DUAL OP AMP

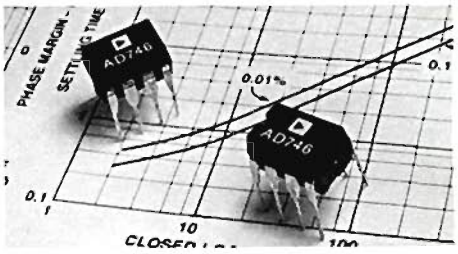
The Monolithic AD746 Is Like Two Matched AD744s

500 ns Settling to 0.01%, 0.0001% THD, 10 μV/°C Max Drift

The AD746† is a dual operational amplifier consisting of two AD744 FET-input op amps on a single chip. Since its introduction in these pages (21-2—1987, pp. 14-15), the AD744's combination of fast ac specs and precision dc performance has set the standard for fast precision bipolar-FET op amps. Now its availability as the only high-speed precision dual FET means savings in parts count and space for such applications as high-performance audio circuitry, active filters, precision buffers for ADCs and DACs, and video display drivers.

AD746's op amps settle to within 0.01% of a 10-volt step in 0.5 μs (0.75 μs max), have 13-MHz (8 MHz min) small-signal gain-bandwidth, 600-kHz full power response, 0.0001% (i.e., −120 dB) total harmonic distortion, and slew rate of 75 V/μs (50 V/μs min for "B" grade).

Performance of the "B" grade device also includes 25°C offset of 0.25 mV (0.5 mV max, and 0.7 mV max over temperature), bias current of 120 pA max, ±10-V CMR of 80 dB min over temperature, and open-loop gain of 175,000 V/V min with 2-kΩ load. Voltage noise is 2 μV peak-to-peak, 0.1 to 10 Hz, and 16 nV/√Hz at 1 kHz.



Crosstalk is typically −120 dB at 1 kHz and −90 dB at 100 kHz. The "B" grade's amplifiers are matched to 0.5 mV max for drift; max bias-current mismatch is 75 pA.

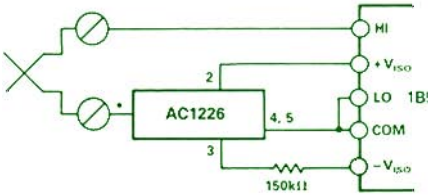
Available grades include J (0 to +70°C), in 8-pin plastic mini-DIP or surface-mount, A/B (−40 to +85°C) and S (−55 to +125°C), in Cerdip. Prices start at $4.25 in 100s.

COLD-JUNCTION COMPENSATOR FOR 1B51

Use Monolithic AC1226 with J, K, T, E, R, S Thermocouples

It Synthesizes Constant-Temperature Reference Junction

The 1B51† Isolated Signal Conditioner for millivolt-level and thermocouple measurements was introduced in these pages earlier this year (23-1, p. 16). Housed in a dual in-line modular package, it has gains from 2 to 1,000 V/V, input offset tempco of ±0.1 μV/°C, 1,500-V rms isolation, and 240-V rms input protection.



*PIN NUMBER DEPENDS ON THERMOCOUPLE TYPE.

Although designed with sufficient gain and stability to handle thermocouple signals, it does not include a means of compensating for the voltage developed at the ambient, or "cold" junction; this compensation will provide a fixed temperature reference. (Note that for low-temperature measurements, the "cold" junction may actually be warmer than the measuring junction.)

The AC1226† is a monolithic cold-junction compensator in an 8-pin mini-DIP, designed to be placed in close proximity to the cold junction. It recreates and subtracts out the effect of ambient temperature variation (0 to +70°C) at the cold junction, *including the nonlinear bow* in the thermocouple characteristic. Powered by the 1B51's isolated front-end power (and drawing only 80 μA), it requires just one external resistor for complete compatibility. Its initial accuracy is to within 0.5°C.

The AC1226 contains a temperature sensor, a buffer amplifier, and a set of resistors, which are brought out to pins and jumpered to provide the correct cold-junction sensitivity to match the thermocouple type. Price of the AC1226 is $7.00 in 100s.

†Use the reply card for technical data.

Updating the Disk Selection Guide

In the last issue (23-3, pages 20-21), we introduced a PC-compatible disk-based component selection guide,[1] to serve as a means of quickly narrowing down the area of product search among the welter of product families, specifications, and grades. A user of op amps, DACs, ADCs, etc., could use the disk to shed light on where to find the areas of greatest payoff to begin a detailed search for a "best buy" using Databooks and data sheets.

The database includes examples of specific grades and package options to enable comparison of individual members of product families, since a lesser grade of a higher-performance family might prove competitive with the premium grade of a lower-performance family—or *vice versa*.

Any catalog is obsolete soon after publication; newer products continually appear. The disk is updated periodically; but meanwhile (you ask) how can I know that the products closest to my needs found on the present disk are still the best choices to consider? Could any newer products be in the running?

This page will summarize for you the new products that have been introduced in *Analog Dialogue* since the most recent disk, M1302-5-6/89 (also known as M1303-1-6/89).

How to Use This Listing: The products in this list are divided into the same categories that can be found on the disk, and the specification columns have the same headings. All products listed in any category appear as they might in a default search of that category, i.e., in order of ascending price in US dollars. Categories not listed are unlikely to have had new commercial-grade products in this period.

After you have performed your search of the disk and found candidates for consideration, look up the same category in this table. Check the products listed for the category to see if there are any that appear competitive and warrant inclusion in your study. Further sources of information on these products[1] are recent Analog Devices Databooks, the latest *Short-Form Designers' Guide*, individual product data sheets, and the footnoted issues of *Analog Dialogue*. If you can't find information on products of interest, call your local sales office or Analog Devices.

DACs—Voltage-Output

Model #	Resolution (Bits)	Settling Time (µs typ)	Interface (0 = serial 1 = parallel 2 = both)	Reference (1 = int. 2 = ext.)	Accuracy Linearity (max LSB)	Price ($ 100s)	Comments
AD7848JN*	12	4	1	1	1	9.85	FIFO, DSP I/F
AD7848KN*	12	4	1	1	0.5	11.40	FIFO, DSP I/F
AD7769JN*	8	4	1	2	2	13.00	2 DACs + 2 ADCs
AD7769KN*	8	4	1	2	1.5	14.05	2 DACs + 2 ADCs
AD7237JN*	12	10	1	1	1	15.00	8 + 4-bit loading
AD7237KN*	12	10	1	1	0.5	17.60	8 + 4-bit loading

DACs—Video

Model #	Resolution (Bits)	Update Rate (MHz min)	Settling (ns max)	Reference (1 = int. 2 = ext.)	Accuracy Linearity (max LSB)	Price ($ 100s)	Comments
ADV476/KN35§	6	35	25	2	0.5	16.00	video graphics
ADV476/KN50§	6	50	20	2	0.5	17.00	video graphics
ADV476/KN66§	6	66	15	2	0.5	20.00	video graphics
AD9712JN & JP*	12	100	30	1	3	40.00	wave generation
AD9713JN & JP*	12	80	30	1	3	40.00	wave generation

ADCs—Video

Model #	Resolution (bits)	Throughput (MSPS)	Full Power Bandwidth (MHz)	Reference (1 = int. 2 = ext.)	Accuracy Linearity (max. LSB)	Price ($ 100s)	Comments
AD9028JE †	8	300	250	2	1	185.00	single out, port
AD9038JE †	8	300	250	2	1	185.00	1:2 demuxed out
AD9028KE †	8	300	250	2	0.8	250.00	single out, port
AD9038KE †	8	300	250	2	0.8	250.00	1:2 demuxed out

[1]Use the reply card to receive a copy.

ADCs—Sampling

Model #	Resolution (Bits)	Convers. Time (µs max)	SHA BW (kHz typ)	Reference (1 = int. 2 = ext.)	Accuracy Linearity (max LSB)	Price ($ 100s)	Comments
AD7872JN‡	14	10	500	1	2	34.00	serial only out
AD7871JN‡	14	10	500	1	2	39.00	serial/par. out
AD1779JN †	14	10	500	1	1	39.00	parallel load
AD1679JN †	14	10	500	1	1	39.00	8-bit bus
AD1779KN †	14	10	500	1	1	43.00	parallel load
AD1679KN †	14	10	500	1	1	43.00	8-bit bus
AD1679JD †	14	10	500	1	1	46.00	8-bit bus
AD1779JD †	14	10	500	1	1	52.00	parallel load
AD1679KD †	14	10	500	1	1	52.00	8-bit bus
AD1380JD‡	16	14	900	1	1	126.00	complete, s/h
AD1380KD‡	16	14	900	1	0.5	152.00	complete, s/h
AD1330KD*	18	10	50	1	0.05%	310.00	18b range, fl. pt.

SAMPLE/HOLD AMPLIFIERS

Model #	Accuracy (%)	Acq. Time (µsec max)	Aperture Time (ns typ)	Aperture Jitter (ns typ)	Price ($ 100s)	Comments
AD1154AW †	0.0015	3.5	80	0.15	42.00	16-bit performance
AD1154BW †	0.00076	3.5	80	0.15	49.50	16-bit performance
AD386BD †	0.00076	3.6	12	0.040	79.00	16-bit performance
AD386TD †	0.003	3.6	12	0.040	99.00	16-bit performance

COMPARATORS

Model #	Prop. Delay (ns max)	Logic (0 = ECL 1 = TTL)	# Chan.	Vos (mV max)	Price ($ 100s)	Comments
AD790JN*	50	1	1	1	2.95	Low power, hi-speed
AD9696KN*	4.5	1	1	3	3.50	Plastic DIP
AD9696KR*	4.5	1	1	3	3.75	SOIC
AD790KN*	50	1	1	0.25	3.95	Low power, hi-speed
AD9696KH*	4.5	1	1	3	4.25	Fastest TTL device, Can
AD9696KQ*	4.5	1	1	3	4.25	Cerdip
AD9698KN*	4.5	1	2	3	6.00	Plastic DIP
AD9698KR*	4.5	1	2	3	6.50	SOIC
AD9698KQ*	4.5	1	2	3	7.50	Cerdip

OP AMPS—Low Input-Current

Model #	Ib (pA max)	CMRR (dB)	Vos (mV max)	Vos TC (µV/°C max)	GBW (MHz typ)	Price ($ 100s)	Comments
AD546JN*	1	90	2	20	1	3.75	plastic package
AD546KN*	0.5	100	1	20	1	4.50	plastic package

OP AMPS—High Speed

Model #	GBW (MHz typ)	Vos (mV typ)	Slew Rate (V/µs typ)	I out (mA min)	Settling (ns to 0.01% typ)	Price ($ 100s)	Comments
AD746JN*	13	0.3	75	5	500	4.25	Dual AD744
AD746BQ*	13	0.25	75	5	500	8.50	Dual AD744
AD843JN*	34	1.7	250	50	135	8.80	CBFET
AD843KN*	34	1.2	250	50	135	13.75	CBFET

ISOLATION AMPLIFIERS

Model #	Peak Voltage (Isol. V)	Gain Range (V/V)	Gain Nonlin. (% max)	Freq. Response (kHz)	Price ($ 100s)	Comments
AD203SN†	1500	10	0.0025	10	58.00	ruggedized

SIGNAL CONDITIONING COMPONENTS & SUBSYSTEMS

1B41AN†	Isolated Signal Conditioner for RTDs In DIP Module
5B38‡	Strain Gage Conditioner for 5B Series
3B20†	Torque Transducer Conditioner for 3B Series

SPECIAL FUNCTION COMPONENTS

AD9901§	200-MHz Digital Phase/Frequency Discriminator
AD7371‡	Voiceband Switched-Capacitor Antialiasing Filter
AD7341‡	Voiceband Switched-Capacitor Waveform Reconstruction Filter
AD9501‡	Digitally Programmable Delay Generator - TTL
AD598†	Monolithic LVDT Signal Conditioner
2S58†	16-Bit LVDT-to-Digital Converter
AD1315*	Active Load with Inhibit for ATE
AD1321*	100-MHz Pin Driver for ATE
AD1322*	200-MHz Pin Driver for ATE

*Described in this issue
†Described in *Analog Dialogue* 23-3
‡Described in *Analog Dialogue* 23-2
§Described in *Analog Dialogue* 23-1

Ask The Applications Engineer—5

High-speed comparators provide many useful circuit functions when used correctly.

by John Sylvan

Question: Why can't I just use a standard op amp in a high-gain or open-loop configuration as a voltage comparator?

You can—if you are willing to accept response times in the tens of microseconds. Indeed, if in addition you require low bias-currents, high-precision and low offset voltages, then an op amp might be a better choice than most standard voltage comparators. But since most op amps have internal phase/frequency compensation for stability with feedback, it's difficult to get them to respond in nanoseconds. On the other hand, a low-cost popular comparator, the LM311, has a response time of 200 ns.

Also the output of an operational amplifier is not readily matched to standard logic levels. Without external clamping or level-shifting, an op amp operating as a comparator will swing to within a few volts of the positive and negative supplies, which is incompatible with standard TTL or CMOS logic levels.

My comparator oscillates uncontrollably. Why does this happen?

Examine the power-supply bypassing. Even a few inches of PC trace on the supply lines can add unacceptable dc resistance and inductance. As a result, transient currents while the output is switching may cause supply-voltage fluctuations, which are fed back to the input through the ground and supply lines. Install low-loss capacitors (0.1μF ceramic capacitors) as close as possible to the supply pins of the comparator to serve as a low-impedance reservoir of energy during high-speed switching.[1]

I've installed bypass capacitors, but I still can't keep my high-speed comparator from oscillating. Now what's the problem?

It could be the comparator's ground connection. Make sure that the ground lead is as short as possible and connected to a low-impedance ground point to minimize coupling through lead inductance. Use a ground plane if possible and avoid sockets.

Another cause of the oscillation may be a high source impedance and stray capacitance to the input. Even a few thousand ohms of source impedance and picofarads of stray capacitance can cause unruly oscillations. Keep leads short, *including the ground clip of your scope probe*. For best measurement results use the shortest possible ground lead to minimize its inductance (<1").

With a slowly moving input signal, my comparator seems to "chatter" as it passes through the transition voltage. Why can't I obtain a single clean transition from the device?

A comparator's high gain and wide bandwidth are typically the source of this problem. Any noise is amplified, and as the signal passes through the transition region, the noise can cause a fast-responding amplifier's output to bounce back and forth. Also, since the device's sensitivity (i.e., *gain*) is higher during a transition, the tendency to oscillate due to feedback increases. If possible, filter the signal to minimize noise accompanying it. Then try using hysteresis which, like backlash in gear trains, requires the input to change by a certain amount before a reversal occurs. For example, after a high-to-low transition on the AD790, its built-in hysteresis requires the input voltage (positive input) to increase by 500 μV to produce a low-to-high transition.

If my comparator does not have internal hysteresis, can I add it externally?

Yes, with external positive feedback. This is done by feeding a small fraction of the output of the comparator back to the positive input. This simple technique is shown in Figure 1. The hysteresis voltage from the lower transition point to the upper transition point will depend on the value of the feedback resistor, R_F, the source resistance, R_S, low output level, V_{low}, and high output level, V_{high}. The low and high transition points are set by:

$$V_{low} \times \frac{R_S}{R_S + R_F} \text{ and } V_{high} \times \frac{R_S}{R_S + R_F}$$

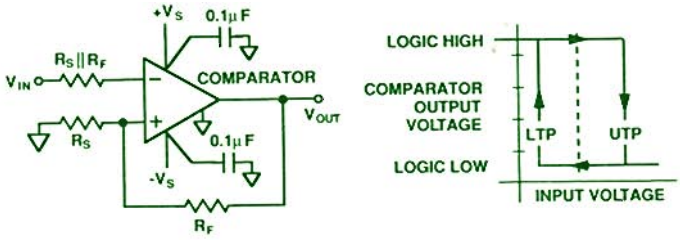


Figure 1. Applying external hysteresis to a comparator.

Figure 2 shows how adding external hysteresis can "clean up" a comparator's response. Figure 2a shows the response of a comparator with bipolar output swing without hysteresis. As the triangular-wave input (trace A) passes through the transition point (ground), the device oscillates vigorously (and couples a portion of the oscillation into ground and the signal-source). Figure 2b depicts the response of the same comparator with 5 mV of external hysteresis applied; it shows a much cleaner transition.

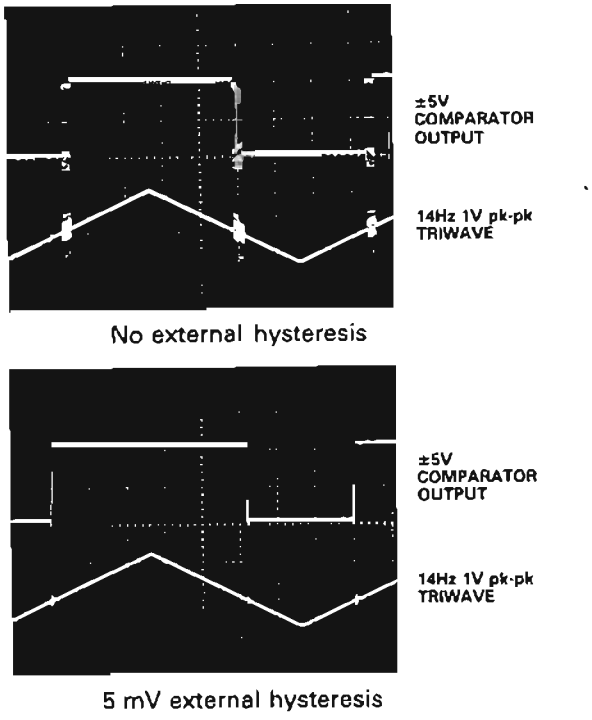


Figure 2. Hysteresis helps clean up comparator response.

[1]A useful discussion of comparator foibles can be found in *Troubleshooting Techniques Quash Spurious Oscillations*, by Bob Pease, *EDN*, September 14, 1989, pp. 152-6

A problem encountered with external hysteresis is that output voltage depends on supply voltage and loading. This means the hysteresis voltage can vary from application to application; though this affects resolution, it need not be a serious problem, since the hysteresis is usually a very small fraction of the range and can tolerate a safety margin of two or three (or more) times what one might calculate. Swapping in a few comparators can help confidence in the safety margin. Don't use wirewound resistors for feedback; their inductance can make matters worse.

What's the difference between propagation delay and prop-delay dispersion? Which of the two specifications is of most concern?

Propagation delay is the time from when the input signal crosses the transition point to when the output of the comparator actually switches. Propagation-delay dispersion is the variation in prop delay as a function of overdrive level. If you're using a comparator in pin-drive electronics in an automatic test system, then prop-delay dispersion will determine the maximum edge resolution. In contrast, propagation delay can be considered as a fixed time offset and therefore compensated for by other techniques.

I have a +5-volt system and don't want to add an additional supply voltage; can I use my comparator with a single supply?

Yes, but to establish the threshold use an adequately bypassed stable reference source well within the common-mode range of the device. The signal level is also to be referenced to this source.

I sometimes see unexpected behavior in my comparator. What could be the cause of this problem?

Examine the common-mode range of the input signal. Unlike operational amplifiers, that usually operate with the input voltages at the same level, comparators typically see a large differential voltage swings at their inputs. If the inputs exceed the device's specified common-mode range (even though within the specified *signal* range), the comparator may respond erroneously. For proper operation, ensure that *both* input signals do not exceed the common-mode range of the specific comparator. For example, the AD790 has a $\pm V_S$ differential input range, but its common-mode range is from $-V_S$ to 2 volts below $+V_S$.

Can you suggest a circuit that performs autozeroing when the comparator is off-line to minimize drift?

Try the circuit shown in Figures 3 and 4. In the Calibrate mode, the input is disconnected and the positive input of the comparator is switched to ground. The comparator is connected in a loop with a pair of low-voltage sources of opposing polarity charging a buffered capacitor in response to the comparator's output state.

If the comparator's minus input terminal is above ground, then the comparator output will be low, the 1-μF capacitor will be connected to the negative voltage (–365 mV) and the voltage from the buffer amplifier will ramp down until it is below the plus input (ground)—plus hysteresis and any offsets—at which point the comparator switches. If it is below ground, the comparator's output will be high, the capacitor will be connected to the positive voltage (+365 mV), the output from the buffer amplifier ramps up. In the final state, each time the comparator switches (when the ramped change exceeds the hysteresis voltage), the polarity of the current is reversed; thus the capacitor voltage averages out the offsets of the buffer and comparator.

At the end of the Calibrate cycle, the JFET switch is opened, with the capacitor charged to a voltage equal to the offsets of the comparator and buffer ± the hysteresis voltage. At the same time, the Calibrate signal goes low, disabling the feedback to the polarity switch and connecting the input signal to the comparator.

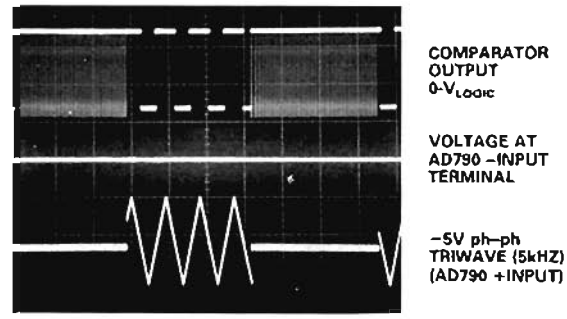


Figure 4. Comparator output, buffer output, and comparator input.

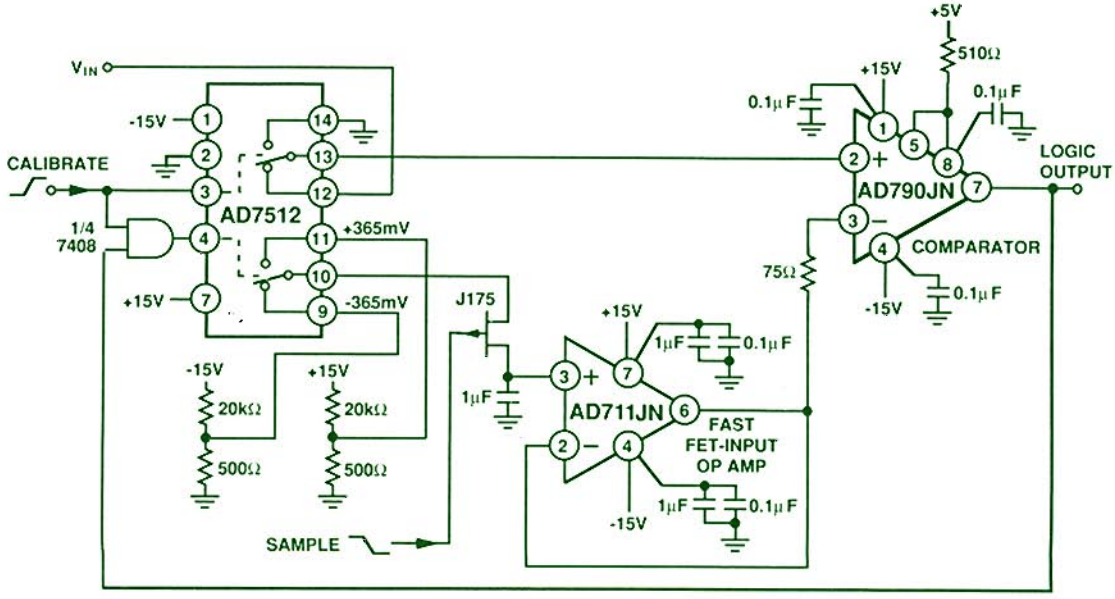


Figure 3. Autozeroed comparator integrates out offsets during calibration cycle.

Worth Reading

Guidelines for Implementing the New Representations of the Volt and Ohm, Effective January 1, 1990 (*Not available* from Analog Devices): From the National Institute of Standards and Technology (formerly the National Bureau of Standards), Technical Note 1263 covers all aspects of the internationally adopted new volt and ohm standards. These new standards, which change the US definition of the volt by +9.264 ppm and ohm by +1.69 ppm, are consistent with SI units and present a common worldwide basis for these units. Order from Superintendent of Documents.

The guideline recommends that measurements with voltage accuracies better than 50 ppm, and resistance accuracies better than 10 ppm, use the new standard; it is optionally recommended for voltage measurements with accuracies to 50-100 ppm and resistance measurements of 10-20-ppm-level accuracy.

For a compact overview of the rationale, implementation, and implications of these new representations, see **"Revised volt and ohm standards,"** *IEEE Spectrum,* July 1989.

APPLICATION NOTES*

Design and Layout of a Video Graphics System for Reduced EMI, by Bill Slattery and John Wynne. 16 pages. A list of "do's and don'ts" for good electromagnetic-compatibility (EMC) design of a video graphics board using Analog Devices video RAM-DACs. Guidelines, testing, and radiation limits of international regulatory bodies on electromagnetic interference (EMI). System noise identification—identifying various sources of noise in a system. PCB layout and design—component placement, multiple-layer boards, grounding, shielding, and filtering components. Practical example of a VGA board design and associated FCC testing.

Animation Using the Pixel-Read-Mask Register of the ADV47X Series of Video RAM-DACs, by Bill Slattery and Eamonn Gormley. 8 pages. Discusses how the pixel read mask register (found on the ADV471, ADV478, and ADV476 RAM-DACs) can be used to provide sophisticated animation with very simple software. A detailed example is given of a C program which produces rotating planets and flyby spacecraft. Of especial interest to graphics designers working in cost-sensitive applications.

An Optimized Radix-4 Fast Fourier Transform (FFT), by Fares Eidi. 24 pages. The FFT is a widely used algorithm for transforming signals from the time domain to the frequency domain and back again. Besides its usefulness as an algorithm for many applications in digital signal processing (DSP), it is also an effective benchmark of performance for DSP processors. This application note describes new programming techniques that yield a very efficient implementation of the FFT. A 1,024-point complex FFT can be calculated in just 2.9 ms, using the ADSP-2100A and ADSP-2101 processors.

Wait State Generation on the ADSP-2100 and ADSP-2100A, by Kapriel Karagozyan. 4 pages. Use the DMACK (data memory acknowledge input) signal to create Wait states for interfacing with slow memory-mapped peripherals. Discusses timing and circuits for generating one or two Wait-states—and logic for multiple-peripheral Wait-state generation.

*Use the reply card to obtain a copy. For a subscription to DSPatch, write to Analog Devices on letterhead.

†Phone Analog Devices Component Test Systems, 1-508-658-9400

SERIAL PUBLICATION

DSPATCH—The Digital Signal-Processing Applications Newsletter,* Number 13, Fall, 1989, 16 pages. It features a new Simulator for the ADSP-2101, offering a new and reconfigurable user interface and a number of new debugging capabilities. Also featured: the Interspec CFM 750, a medical diagnostic imaging device using Doppler sonar to do color blood-flow mapping; its numbers are crunched by the ADSP-1110A 16 × 16 single-port multiplier-accumulator (MAC) in a 28-pin DIP with a 40-bit-wide accumulator. An applications feature describes error-reducing Huffman coding (used in facsimile machines), and shows how simply it can be done with the ADSP-2100, making use of its complete barrel shifter. Also included are Q and A, "How to talk analog" (reconstruction filters), a DSP activities update, and a listing of available DSP literature.

BROCHURES

LTS-2020 Component Test Systems now featuring mixed-signal capability. † Describes the LTS-2020 and the many types of tests it can perform: DACs, ADCs, linear circuits, SSI/MSI digital devices, discrete devices (high voltages and currents), smartpower, analog switches/multiplexers, and mixed-signal devices.

The 6B Series One-Step Sensor-to-Host Signal Conditioning—Complete, Configurable, Computer-Ready.* Describes the 6B Series of modular sensor-to-serial converters announced in Analog Dialogue 23-1.*

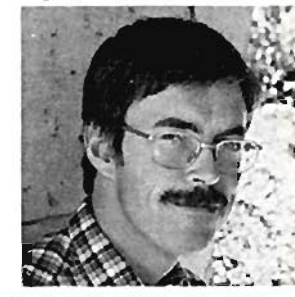
REPRINTS AVAILABLE*

"Advances in PC-Based Data Acquisition," by R. Joyce, from *American Laboratory*, June, 1989. 4 pages. Describes the use of data-acquisition plug-in boards for PCs, with specific reference to the triggering and multiplexing capabilities of the RTI-860.

"Signal Conditioners Link Sensor to Serial Port," by Jane M. Stoffel, *Control Engineering*, September, 1988. Describes the 6B Series signal conditioners (see above).

"Putting Anti-Lock Braking to the Test," from *Sensors*, February, 1989. 2 pages. (reprint *not* available) Describes a testing program currently being conducted for a major U.S. automotive manufacturer to evaluate the performance of an anti-lock braking system (ABS). Includes transducers, signal conditioning, calibration mode, computer, analog input board, software, analytical capabilities, and benefits.

MORE AUTHORS *(continued from page 2)*



John Wynne (page 17) is Applications Engineering Manager at Analog Devices BV, Limerick, Ireland. Previously he was a Design Engineer at Sperry Gyroscope's Avionics Division in the United Kingdom. He has published a number of articles in various publications.

John Sylvan (page 20), a Senior Technical Publicity Specialist at Analog Devices, in Norwood, Massachusetts, has written many articles for a variety of technical publications. His photo and a biographical sketch appeared in volume 23, number 1.

Bob Clarke (page 13) is a Product Marketing Engineer in the Linear Group at Analog Devices Semiconductor. His photo and a biographical sketch appeared in volume 23, number 3.

Potpourri

An Eclectic Collection of Miscellaneous Items of Timely and Topical Interest. Further Information on Products Mentioned Here May Be Obtained Via the Reply Card.

IN THE LAST ISSUE

Volume 23, Number 2, 1989, 24 Pages

ERRATA . . . ***Analog Dialogue*** 23-3, page 21, Fig. 4: Because of pricing errors in the database, AD573JD is shown above AD573JN. Actually, it should follow AD575JD; similarly, AD573KD should follow AD575KD . . . In the 1988 and 1989-90 Converter Products Databooks, the D-22 package, specified for AD9700BD/BW/SD and AD9701BQ/SQ, has wrong dimensions. Use the data-sheet information . . . AD9028/9038 data sheet, in ENCODE INPUT section: for lines labeled Pulse Width (High)' and Pulse Width (Low)', data is transposed . . . Early editions of the ADSP-2100 Cross Software Manual and the ADSP-2100 User's Manual- give an erroneous phone number for bulletin-board service. The correct number is **(617) 461-4258**, 8 data bits, no parity, 1 stop bit, 300 to 2400 baud . . . 6B Series March 1989 Ordering Guide, page 2, power-supply nominal voltage spec (omitted) is 5 volts.

PRODUCT NOTES . . . New Data Sheets. A new ADSP-2100/A data sheet is available. Highlights include the ADSP-2100AU 12.5-MHz-over-MIL-temp grade, 100-pin CQFP package for MIL grades, and a minor change in DMACK specs. . . . **Other:** Two 2-page Product Notes are available for the 3B Series: "Dimensional Gaging Measurement with LVDTs and the 3B17" and "In-Vehicle Testing," with RTI-800 Series data-acquisition boards . . . The AD588 Voltage Reference is now available in a 20-pin LCC package . . . The LTS-1906 Thermonics Interface Package, coupled with the Analog Devices LTS-2020 Component Test System, provides a capability for testing devices over the full military temperature range. For information call ADI Component Test Systems, (508) 658-9400 . . . Many ADI plastic surface-mount devices are available in large quantities with tape and reel packaging. CWYLSO* . . . An Ordering Guide is available for the µMAC-1050 (see page 10). DOS drivers are available for using the µMAC-1050 with PC-based application programs, written in such languages as Microsoft C, Microsoft interpreted-, compiled-, and quick BASIC, and IBM interpreted BASIC . . . An evaluation board is available for the AD9028 300-MSPS 8-bit ADC.

PATENTS RECEIVED . . . 4,808,908 to A. Paul Brokaw and Stephen Lewis for Curvature Correction of Bipolar Bandgap References . . . **4,811,296** to Douglas Garde for Multi-Port Register File with Flow-Through of Data . . . **4,857,862** to A. Paul Brokaw for High-Gain IC Amplifier.

UPDATE . . . A variety of lower-priced IBM-PC cross-software packages are available for the ADSP-2100A and the the ADSP-2101. CWYLSO* . . .The following CMOS products are now available in Cerdip packages (Q), replacing the equivalent side-brazed ceramic package (D): AD7240SD; AD7520JD; AD7521UD; AD7522TD; AD7525TD/+; AD7542AD,BD,AD/+,BD/+,SD,TD,SD/883B,TD/883B; AD7543AD/+,SD/883B,GTD. For further details, CWYLSO.* . . . Price has been reduced on the AD770 8-bit 200 MSPS monolithic flash ADC. CWYLSO* . . . SHOWS: We will be at SAE in Detroit, Feb. 26 to March 2; Southcon in Orlando, March 20-22, and ICASSP in Albuquerque, April 3-6. If you're planning to attend, come see us . . . **DSP Service Notes:** Our DSP Applications assistance hotline can be reached at (617) 461-3672.

*CWYLSO = Check with your local sales office.

ANALOG DEVICES

Complete 12-Bit A/D Converters

AD9003/AD9005

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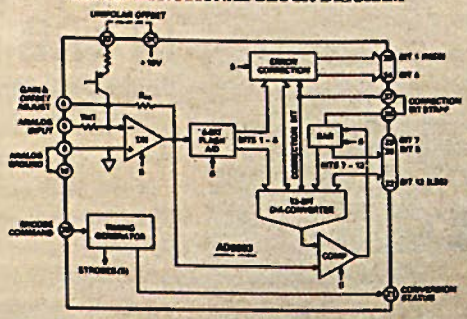
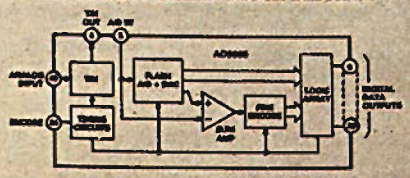
AD9003
- 12-Bit, 1 MSPS Word Rates
- T/H and Timing Included
- Single 40-Pin DIP
- −80 dB Harmonics
- 70 dB SNR
- ±0.5 LSB Differential Linearity
- ±0.8 LSB Integral Linearity

AD9005
- 12-Bit, 10 MSPS Word Rates
- T/H and Timing Included
- Single 48-Pin DIP
- −72 dB Harmonics
- 64 dB SNR
- TTL-Compatible
- Offset Binary Output

AD9003 FUNCTIONAL BLOCK DIAGRAM



AD9005 FUNCTIONAL BLOCK DIAGRAM



AD9003 DESCRIPTION

The AD9003 A/D Converter is a complete 12-bit, 1 MSPS analog-to-digital converter which combines low cost and high performance in a single 40-pin DIP. The unit includes track-and-hold (T/H), timing, and encoding functions with a power dissipation of only 2.2 watts.

This TTL-compatible device is capable of converting analog signals to the Nyquist limit at encode rates through 1 MSPS. Its 1-µs conversion interval includes acquisition time for the internal T/H, making it a true megasample-per-second converter.

Proprietary conversion techniques achieve linearity equivalent to the best successive approximation ADC along with subranging conversion speeds. A conversion status signal simplifies transferring output data into system logic. Innovative thick- and thin-film technologies assure excellent performance over temperature without compromising ac characteristics.

The AD9003KM operates at case temperatures from 0 to +70°C; the AD9003SM and AD9003TM units operate from −25°C to +100°C.

AD9005 DESCRIPTION

The AD9005 A/D Converter is a complete 12-bit analog-to-digital converter featuring on-board track-and-hold (T/H), voltage reference, and timing circuits.

High speed and high resolution are combined by using subranging converter architecture. Signal-to-noise ratios of 67 dB at 540 kHz inputs and 65 dB at 2.3 MHz inputs remain at 64 dB SNR when the input is 4.3 MHz.

This kind of performance is made possible by using advanced bipolar integrated circuits, custom designed for the AD9005 and manufactured by Analog Devices.

Despite its extraordinary combination of high speed and high resolution, the AD9005 dissipates only 3.1 watts. This characteristic and its small size make it extremely attractive for applications in which power or space are at a premium.

Commercial devices operate from 0 to +70°C case temperatures as model AD9005TM; the model AD9005TM covers the military range of −55°C to +125°C.

TO TRACK COMPLETE 12-BIT HIGH-SPEED A/Ds, HOLD ON TO THIS PAGE.

If tracking down complete, high performance 12-bit A/D converters is a problem, get a hold of our new AD9005 and AD9003. They completely eliminate the need for external support circuits. Because both contain track-and-hold, timing, reference circuits, and everything else needed to perform the digitizing function.

For guaranteed ac and dc performance, the AD9005 is the top choice. Signal-to-noise, harmonic distortion, and differential and integral nonlinearity are 100% tested. Harmonic suppression is typically 75 dB at 540 kHz, and 72 dB at 2.3 MHz and 4.3 MHz. The AD9005 offers 10 MSPS encode rates and dissipates only 3.1 watts. And to simplify assessing performance, an AD9005 evaluation board is available.

For applications requiring 12 bits at 1 MSPS, you'll get unparalleled linearity and low power dissipation in the AD9003. And its ac performance is verified with digital signal processing. The AD9005 and AD9003 come in with the right performance, the right specs, and the right prices.

To track down more information, get a hold of applications help at (919) 668-9511, or call your nearest Analog Devices office.

ANALOG DEVICES

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